An All CMOS, 2.4 GHz, Fully Adaptive, Scalable, Frequency Hopped Transceiver

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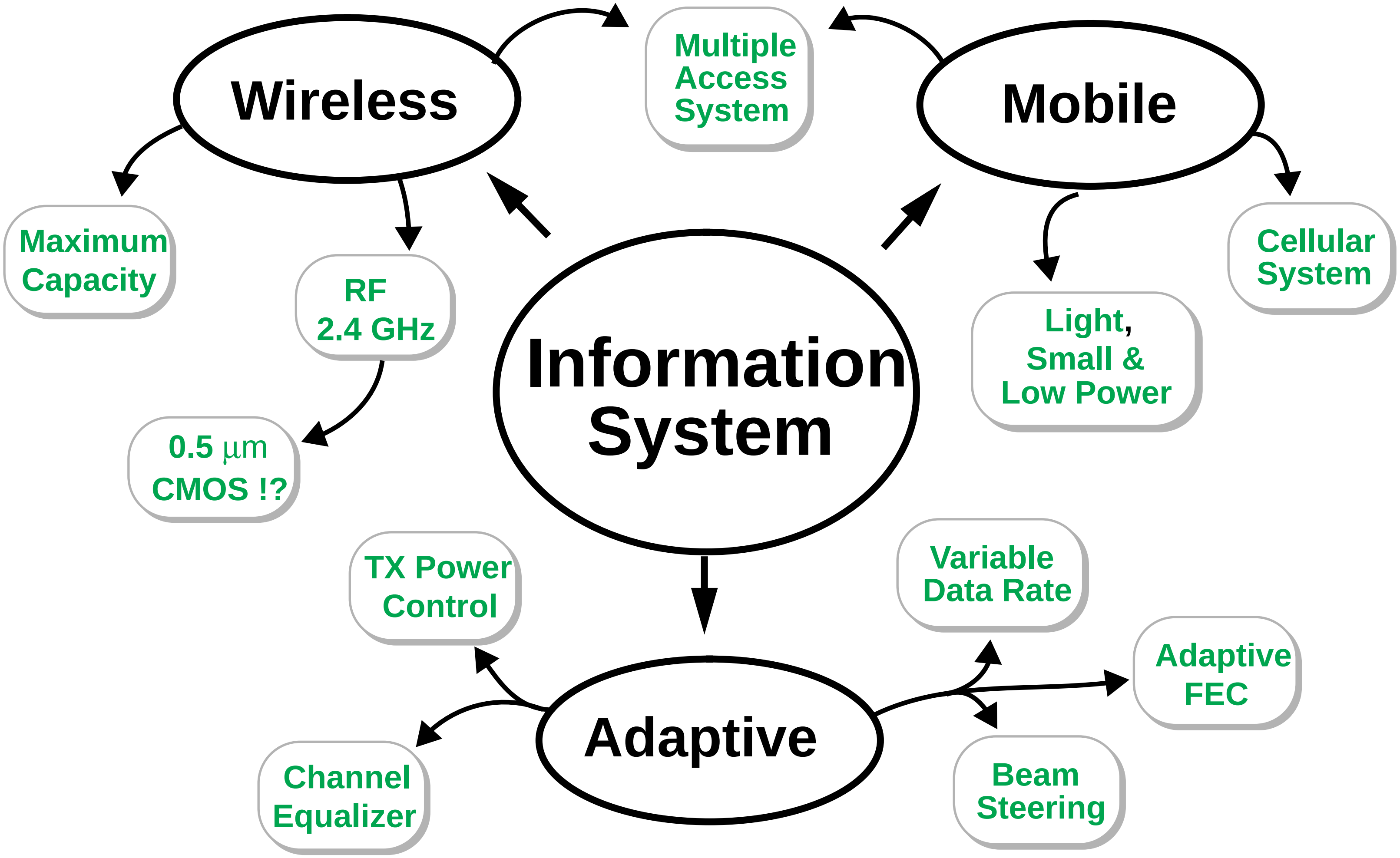
WAMIS II


Wireless
Multiple Access System
Mobile
Maximum Capacity
RF 2.4 GHz
0.5 µm CMOS !?
Information System
Light, Small & Low Power
Cellular System
TX Power Control
Variable Data Rate
Adaptive FEC
Adaptive
Channel Equalizer
Beam Steering

System Descriptions

- Wireless LAN.
- Mobile and Wireless (RF), ISM band : 2402 MHz to 2482 MHz.
- Adaptive data rate : 1 Mb/s → 48 Mb/s
  - Symbol rate:
  - Band Width :

500 KBaud 625 KHz	**or**	2 MBaud 2.5 MHz	**or**	8 MBaud 10 MHz

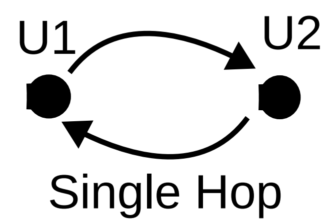
  - Modulation:

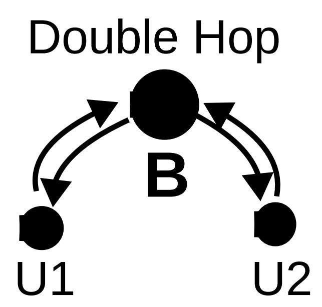
4-QAM 2 bits/Symbol	**or**	16-QAM 4 bits/Symbol	**or**	64-QAM 6 bits/Symbol

  - Adaptive Beam Steering.

System Descriptions (Continued)

- Transmit power control.
- Frequency hop to decrease power density (FCC regulation) and provide frequency diversity.
- Single hop (peer to peer) system.
- Use every channel in each cell (and not every other channel).



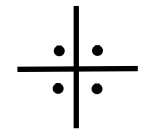


Effects of System Spec on System Design
1 - Adaptive Data Rate

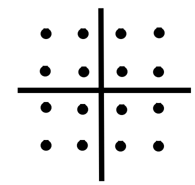
- 4-QAM to 64-QAM modulation:

Table 1:

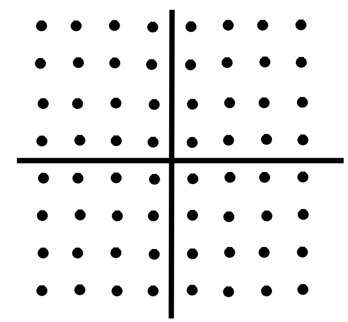
Modulation	Signal Levels (I & Q)	Max/Min Power	Dynamic Power (dB)	SNR @ BER=1E-6
4-QAM	± 1	1/1	0	13.5 dB
16-QAM	± 1,3	9/1	9.5	20.4 dB
64-QAM	± 1,3,5,7	49/1	17	26.5 dB



4-QAM



16-QAM



64-QAM

- System issues: 64 QAM → High linearity + Low noise
  → High dynamic range.

2 - Beam Forming Idea

$S_{Ra}=0$: Received **out-of--phase**
$S_{Rb}=2.S_{R1}$: Received **in-phase**

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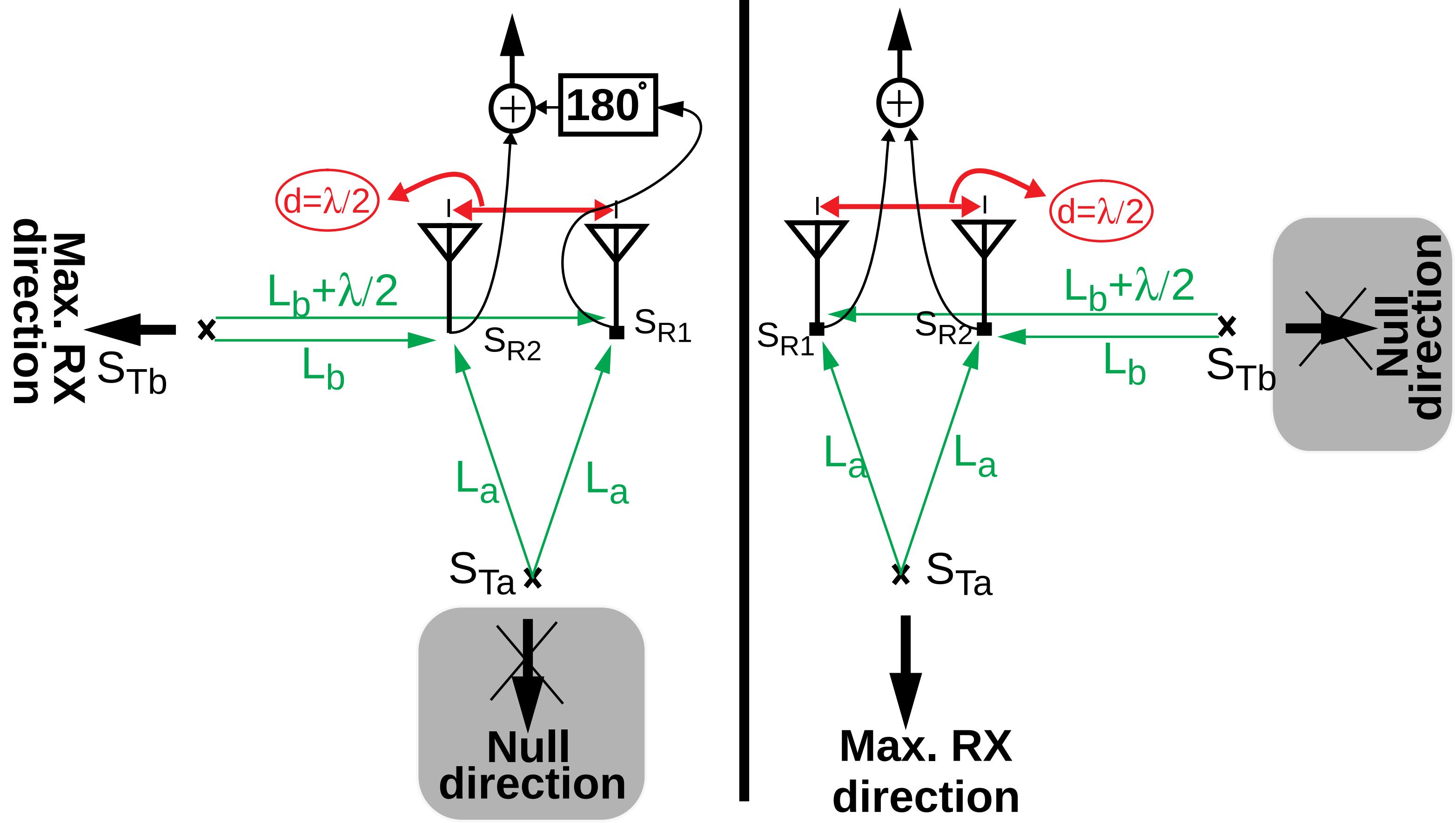
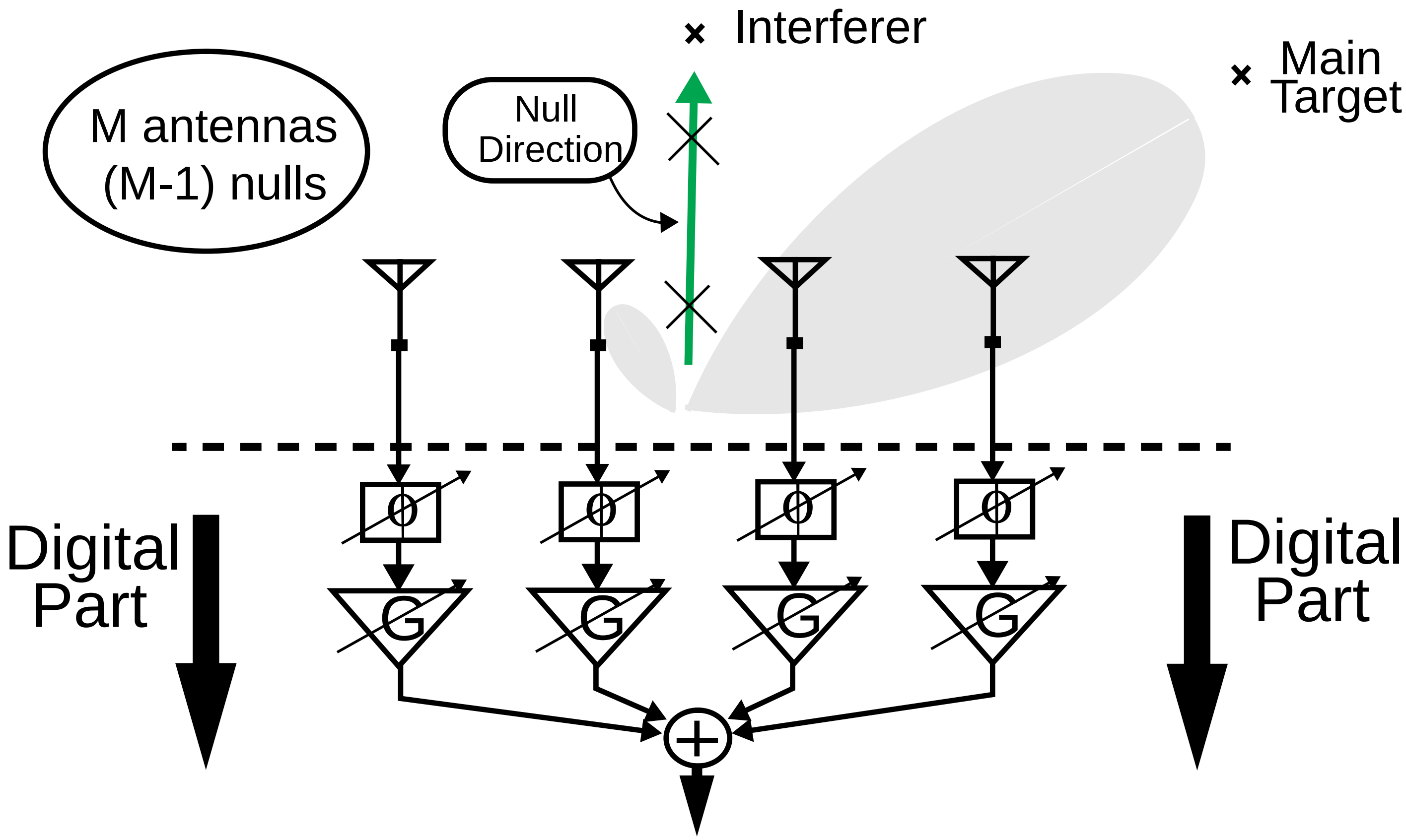
$S_{Rb}=0$: Received **out-of-phase**



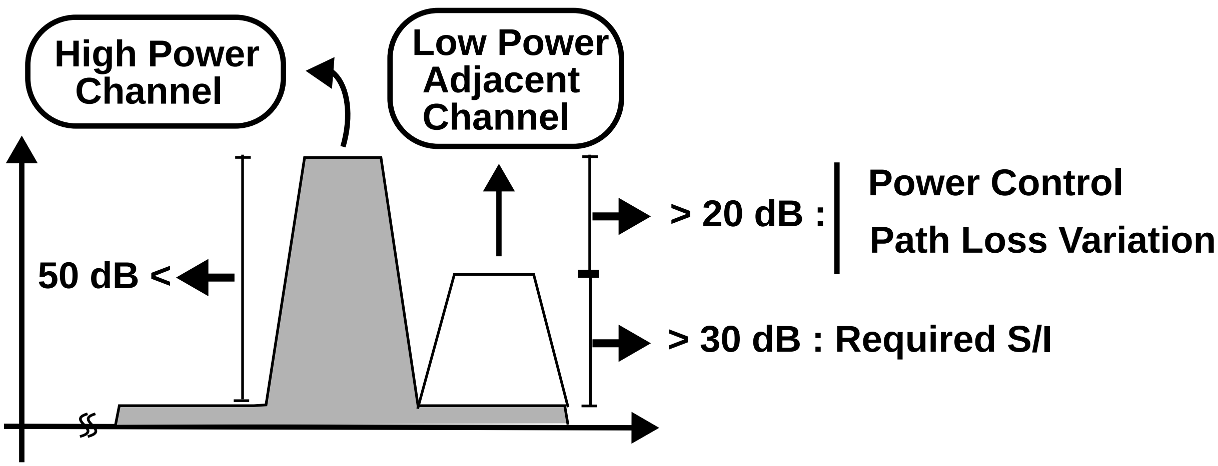
2- Beam Forming (Continued)



- Beam direction is electrically set by adjusting gains and phase shifts.
- Reduces the interference and multipath.
- Requires duplicate analog branches (the same number as antennas).
- Isolation problem between paths.

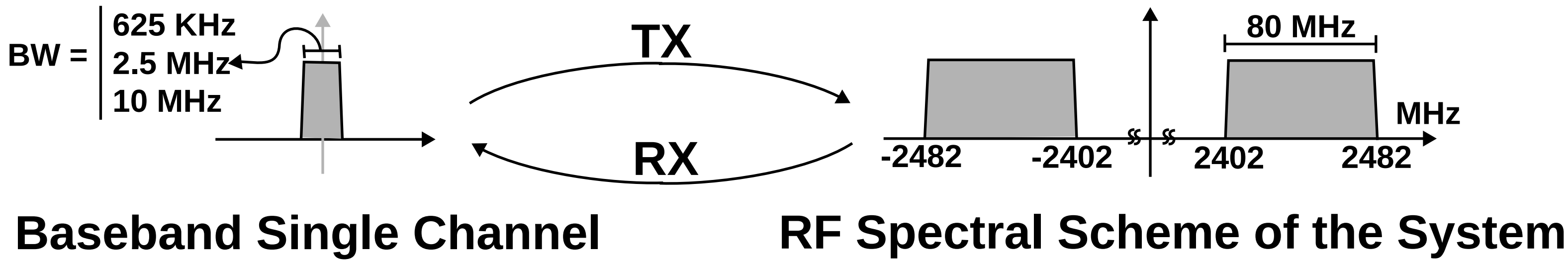
3- Power Control & Use of Every Channel in Each Cell

- **Maximum capacity → Power control > 30dB.**
- **Use of every channel → Very low off-channel leakage (< 50 dB).**



- **With maximum average output power = 20 mW and maximum peak output power =110 mW (64-QAM), the above requirement makes the power amp. difficult to design (low efficiency).**

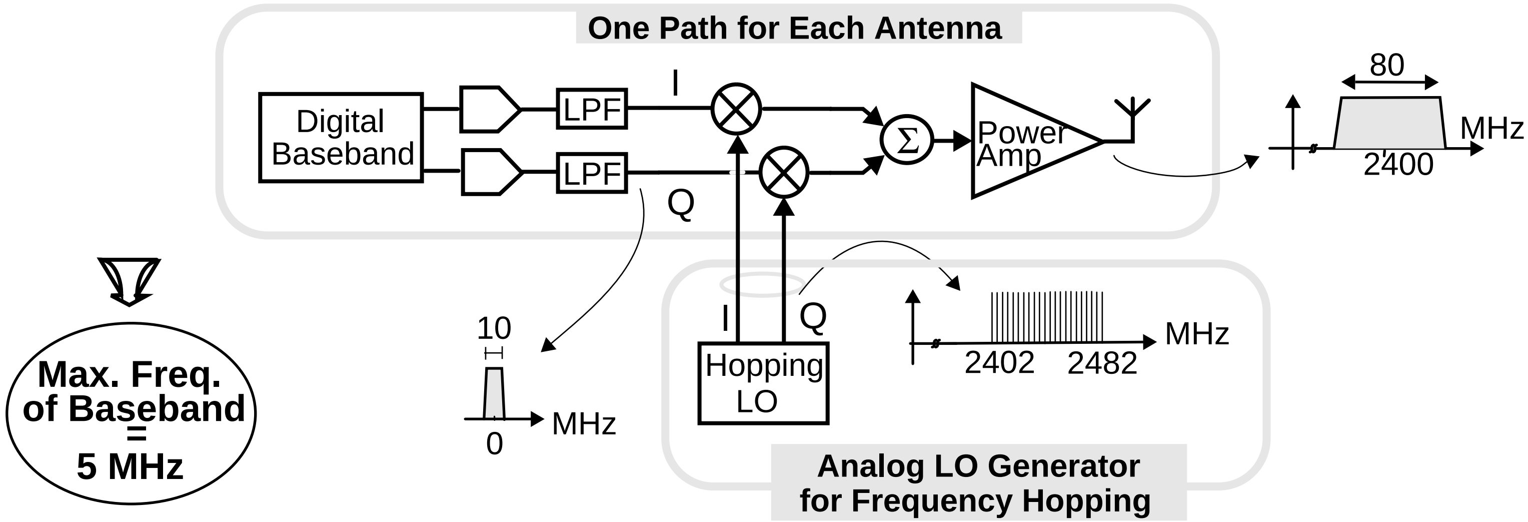
General Strategy of the Design



- Simplified circuitry in the signal path.
  - One Step up-conversion.
  - Two step down-conversion with heavy passive filtering for image rejection.
  - Not very high frequencies at the boundary of analog and digital sections (CMOS A/D and D/A).
  - Very few off-chip component.
- Push all the complexity to the LO generation stage.

Transmitter Architecture

Direct Up-conversion & Analog Frequency Hopping



- Highly integrated, minimum off-chip components, highly reliable
- No out-of-channel image and LO leakage.
- RF fast frequency hopping.

Transmitter System Specs

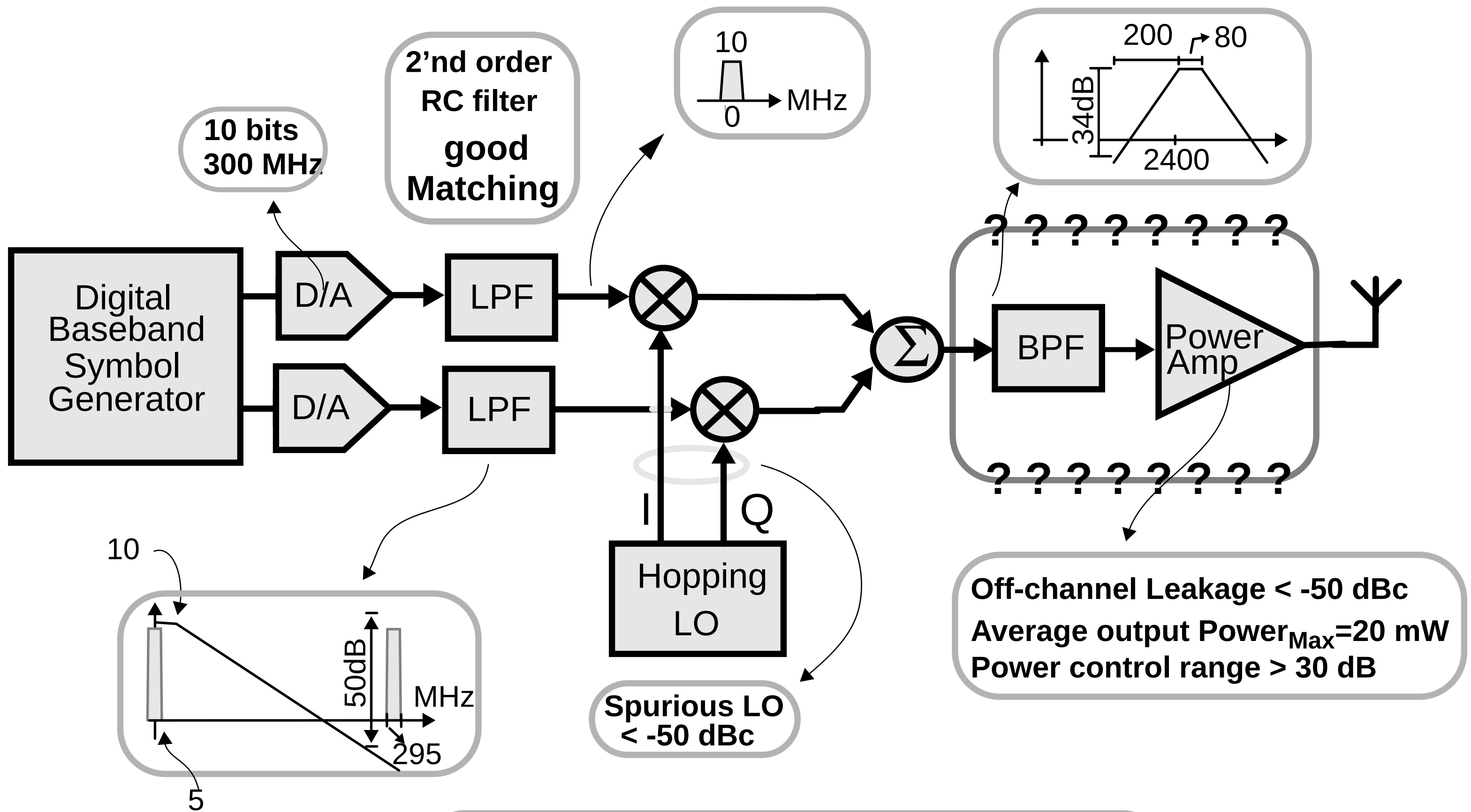
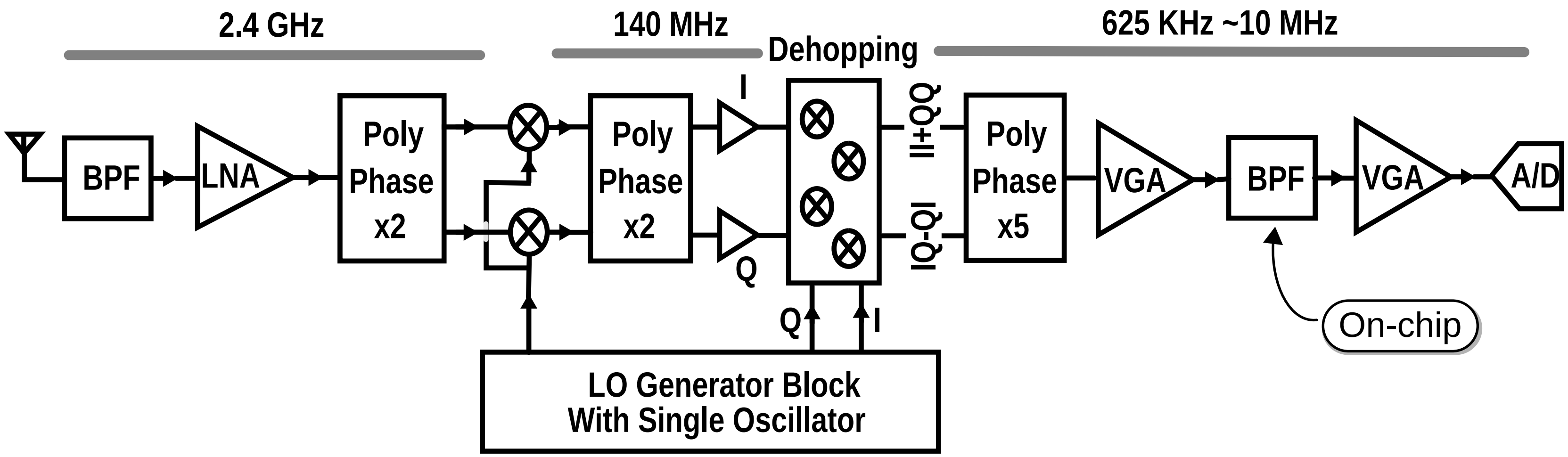


Image Rejection > 40 dB

Receiver Architecture
Double-IF Downconversion

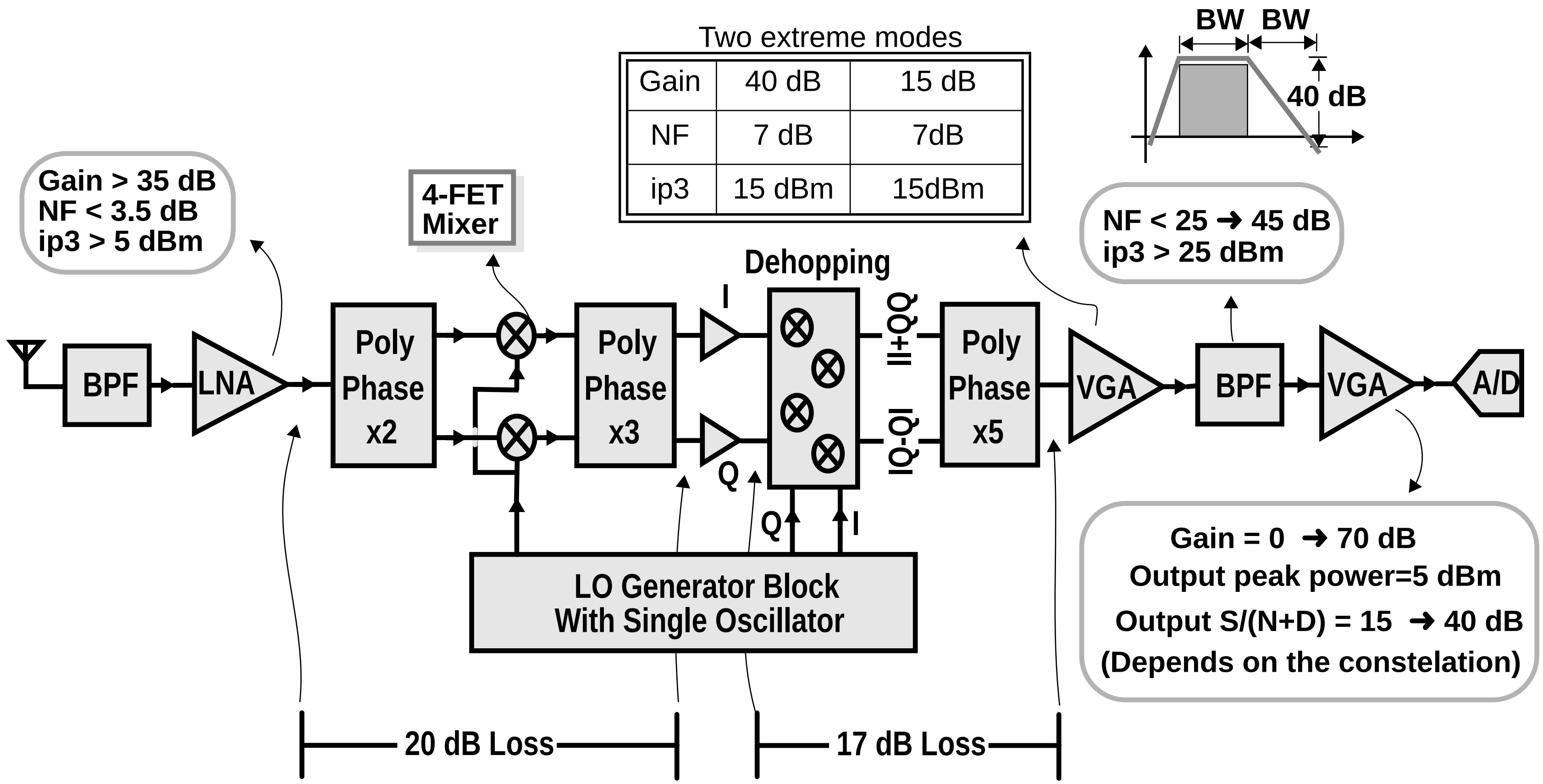


- Two steps down conversion.
- 1st IF frequency dehopping.
- RF image rejection = 33 dB (RF filter) + 35 dB (Quadrature image rej.)
- 50~60 dB image rejection at first IF.
- On-chip power adaptive IF filtering.

Preliminary Receiver System Specs

Two extreme modes

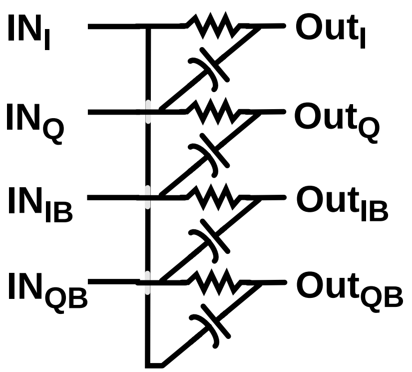
Gain	40 dB	15 dB
NF	7 dB	7dB
ip3	15 dBm	15dBm



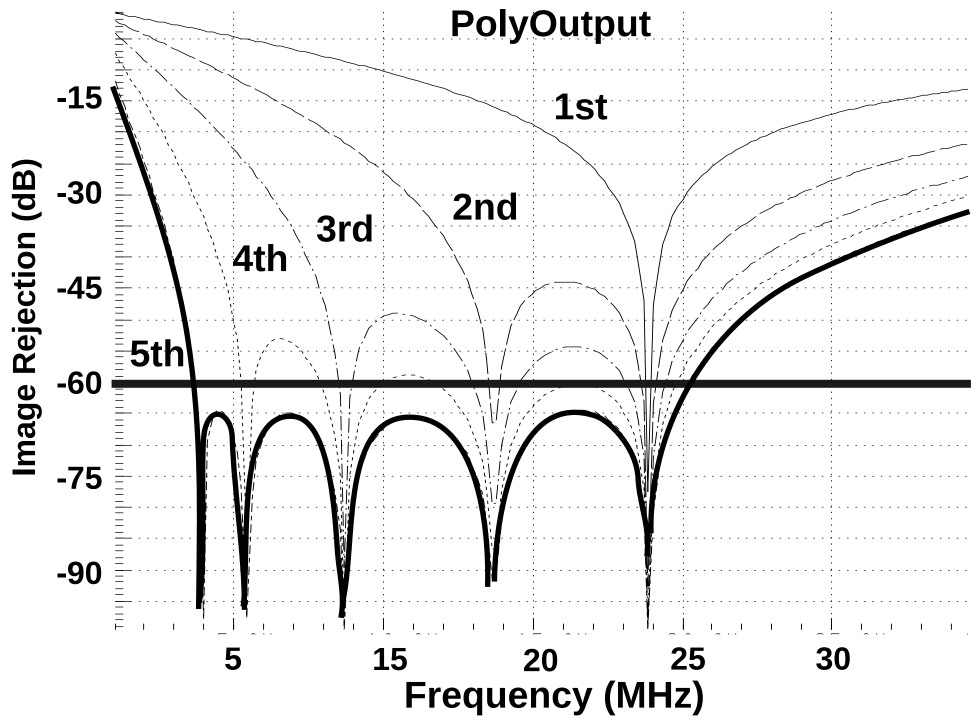
- **RX NF = 6 dB**
- **RX input ip3 = -10dBm**

Wideband Polyphase Filters

Staggered polyphases



5 stages of polyphase in cascade with different center frequencies



- **Wideband image rejection can be obtained with staggering several polyphase stages.**
- **Loss of the N polyphase stages is (N-1)x3 dB.**
- **The wider the polyphase, the more lossy it is.**
- **For 60 dB image rejection, 0.1% matching between polyphase components is required.**

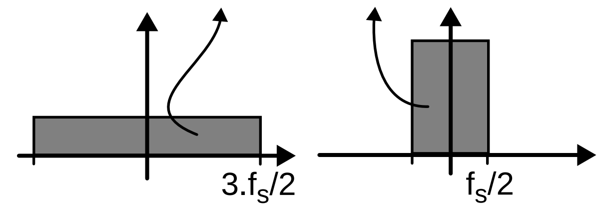
Supporting Variable BW

- **Off-chip SAW filter bank:**
  - **Requires off-chip components (6 for each path!), UNACCEPTABLE.**
- **Using oversampling properties:**
  - **Constant A/D clock frequency (40 MHz).**
  - **Constant IF BPF bandwidth, 10 MHz (4 time oversampling).**
  - **Lower signal BW ➜ Higher oversampling rate ➜ Lower noise density.**
  - **Excess BW in BPF ➜ High interference.**
  - **Noise reduction ≅ Interference increase ➜ Constant dynamic range.**
  - **Requires complicated digital front-end.**
- **Variable BW BPF:**
  - **Requires Variable BW analog BPF.**
  - **Switch capacitor filter for easy BW scaling.**

Oversampling and Resolution Trade-off

- **Total quantization noise power** $= \frac{1}{12} \cdot \left(\frac{V_{max}}{2^n}\right)^2$
- **Total quantization noise is independent of sampling frequency.**
- **Quantization noise density inversely proportional to the sampling frequency.**
- **With a constant signal bandwidth:**

Equal total quan. noise → Equal areas



Noise Power density $\propto \frac{1}{\text{Sampling freq.}}$

Sampling Freq. $\Uparrow \rightarrow$ **Total Quantization noise** $\Downarrow \rightarrow$ **Resolution enhancement**

4 times oversampling ⟷ **6 dB noise improvement** ⟷ **1 bit of Resolution**

Large Bandwidth at the A/D Input

- Bandwidth more than a channel passes interference.
- Having equal power at adjacent channels:

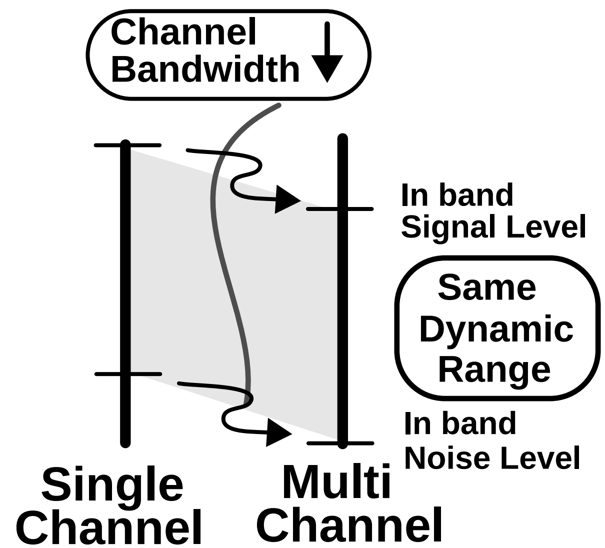
4 times Bandwidth ≈ ⟷ **4 times Interference** ⟷ **6 dB Loss In (S/I)**

- With a fixed filter bandwidth and sampling frequency:
  - Channel bandwidth reduction increases the over sampling rate :

In-band noise reduction gains some LSBs.

  - Out-of-band interference decreases:

S/I degradation loses same Number of MSBs.



➡ **Unchanged dynamic range**

Omitting Off-chip Filter Bank

Post Signal Processing

1 - A fixed on-chip analog 10 MHz BW at 40 MHz.

2 - **Exchange**

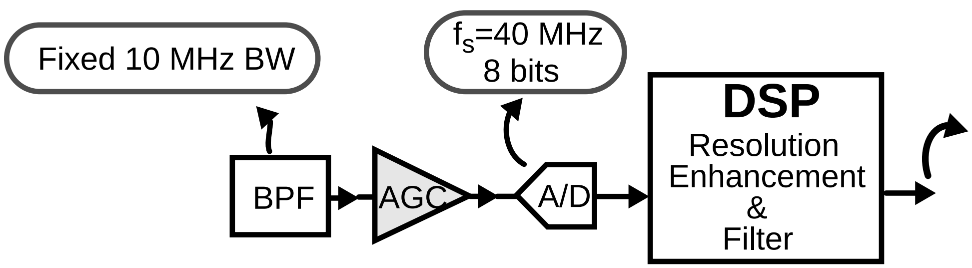
Oversampling ⟷ Resolution

A/D

f_s=40 MHz
8 bits

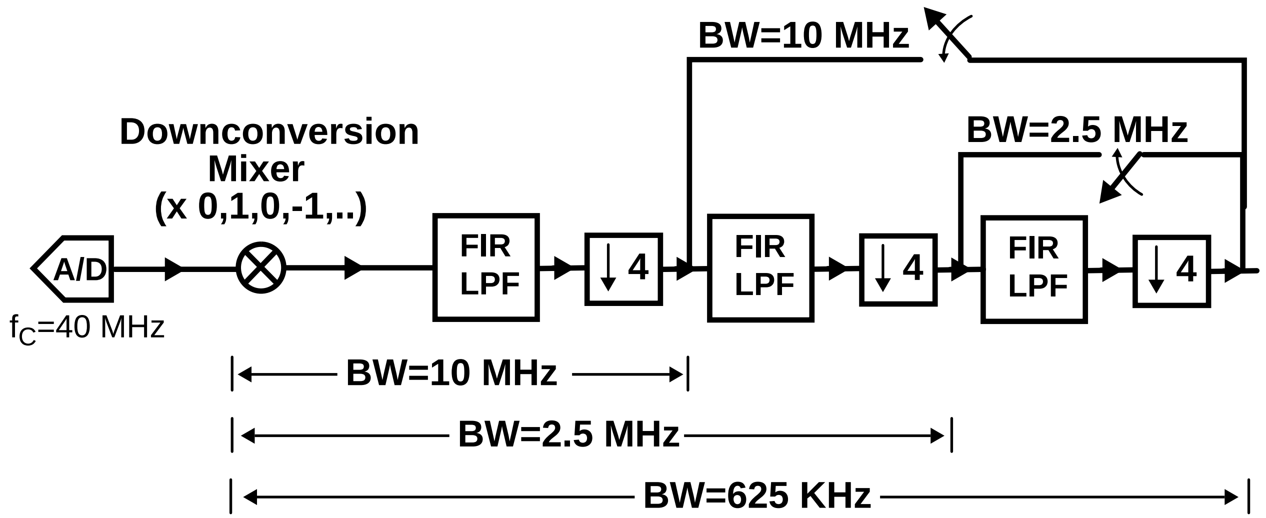
BW	Oversampling Ratio	Desired/Total Power in 10 MHz BW	Final resolution *Without* Noise Shaping
625 KHz	64	16 (12 dB)	11 bits (66 dB)
2.5 MHz	40	4 (6 dB)	10 bits (60 dB)
10 MHz	4	1 (0 dB)	9 bits (54 dB)

Cancel Out



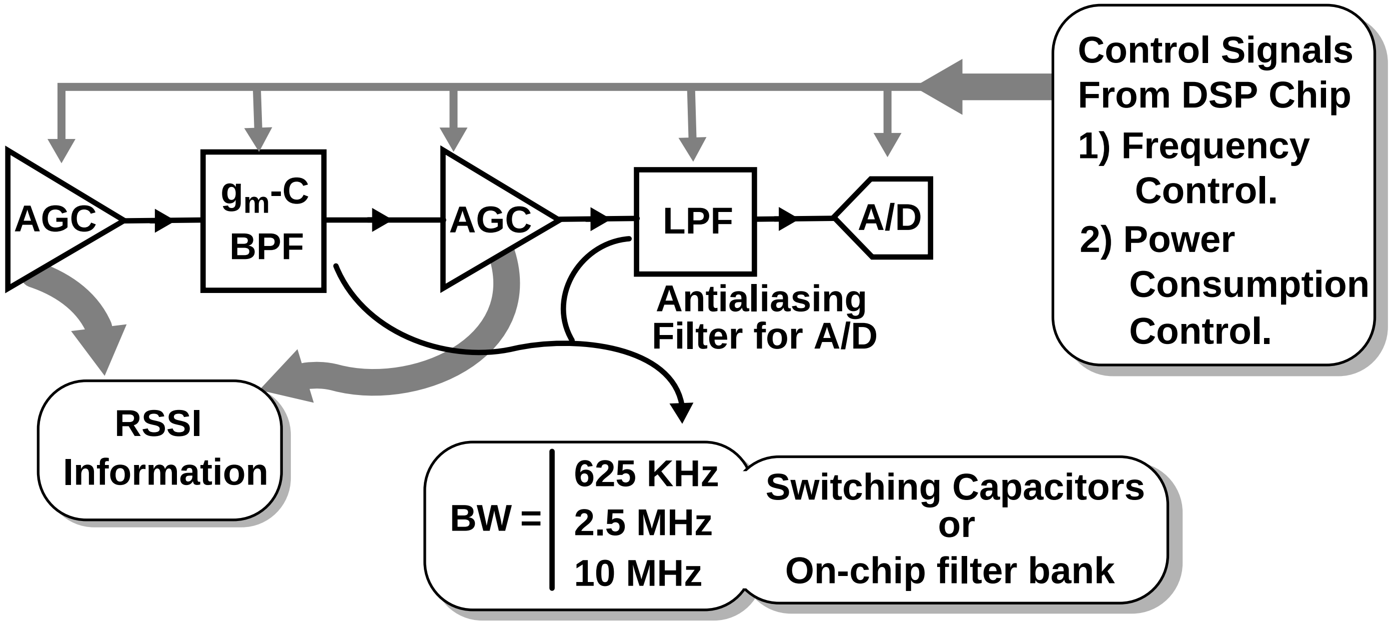
9 bits Resolution/Channel
Independent of BW

Required Digital front-end for Extracting Oversampling Enhancement



- **Complicated digital front-end.**
- **Increases the power dissipation and area of the digital chip.**

Variable Bandwidth Analog BPF

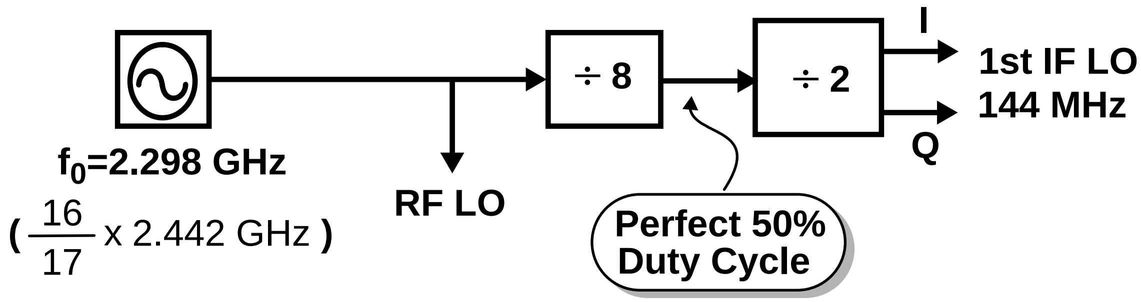


- BW and center frequency of the g_m-C BPF scales with switching filter capacitors.
- Capacitors and the power consumption of the IF g_m-C filter are tunable.
- Large desired signal ➜ Smaller g_m, higher noise, and lower power dissipation.
- A/D power dissipation and number of bits can be optimized for each BW and constellation.

Adaptive Power Consumption
Consumes Minimum Power in any Condition

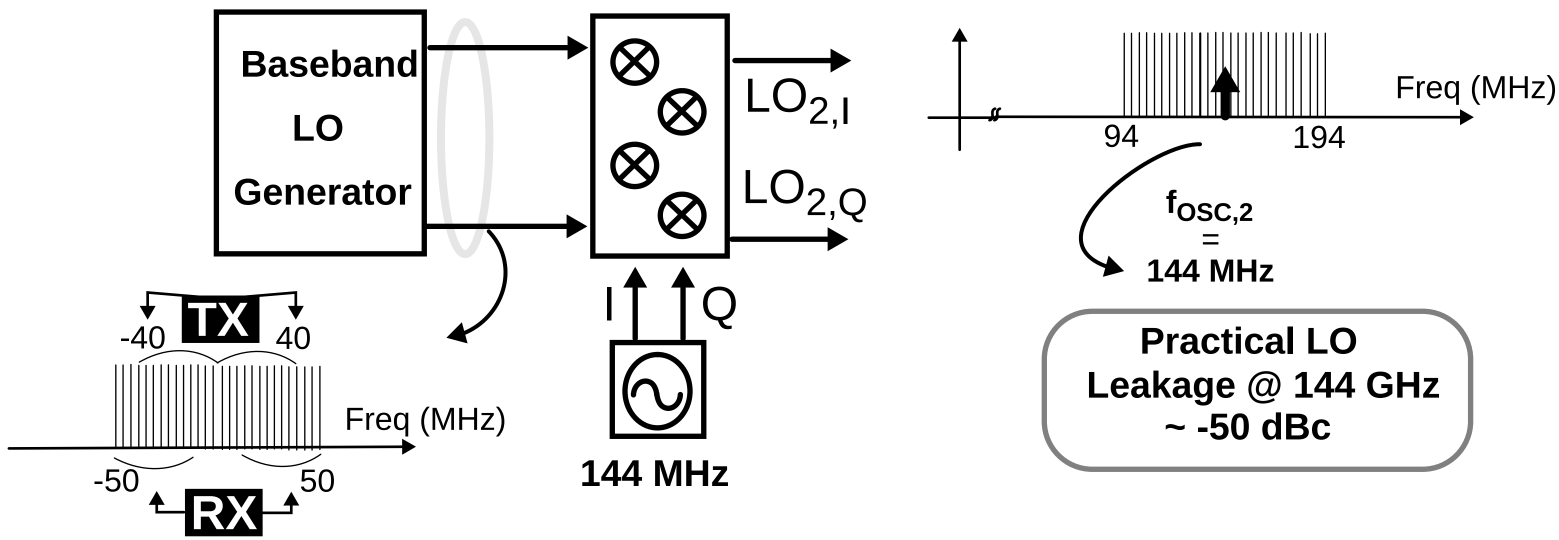
LO Signal Generator

Single VCO for generating two LO's



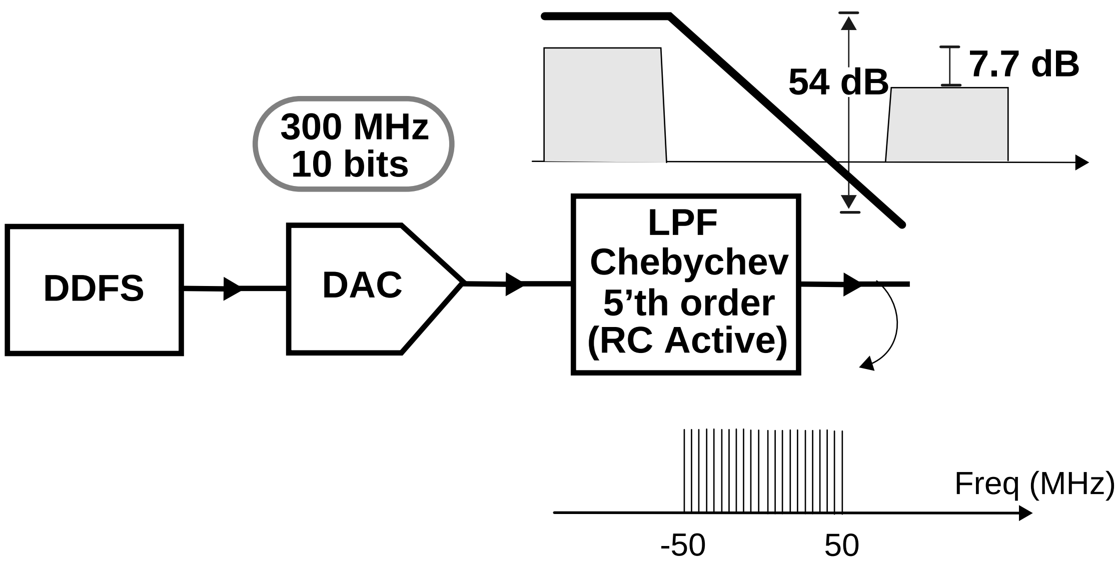
- **Fixed frequency VCO (channel selection is done with DDFS).**
- **Single VCO is used to generate both LO signals.**
- **Prevents problems of multiple VCO on chip.**
- **A divide by 16 stage can provide precise quadrature LO's at 144 MHz.**
- **Dividers are part of the synthesizer and don't have overhead on the system.**

LO Signal Generator
For Fast Frequency Hopping



- **100 MHz Bandwidth.**
- **LO hops over the whole bandwidth with high hop rate.**
- **DDFS should be used for hopping rather than PLL.**
- **Spurious signals should satisfy the in-band and out-of-band leakage specifications: LO leakage & Side-band < -50 dBc**
- **Precise Quadrature LO at the output.**
- **Hard switched MOS switches provide good matching in the mixers, and thus, good unwanted sideband suppression in LO.**

Baseband LO Generator Schemes



- Very high frequency CMOS DAC is required.
- C-T filters should be used as smoothing filters.
- Characteristic of I & Q filters should be highly matched.

Circuit Ideas

Power Amplifier Issues

- **Specifications:**
  - Maximum output power = 20 mW
  - Off-channel leakage < -50 dBc
  - Power control > 30 dB
- **General methods:**
  - Pre-distortion circuits to compensate the non-linearity.
  - Use closed loop techniques to measure the non-linearity and compensating it.
  - Simple linearizing techniques.
- **Performance criteria:** Efficiency.

Very high RF frequency → **The simpler the technique = The better it works**

Power Amp: (Continued)

- **Examining the basic CMOS linearity properties.**
  - Device input characteristics:
    - High bias voltage for V_{GS} is desired.
    - With V_{GS} (bias) = 2:

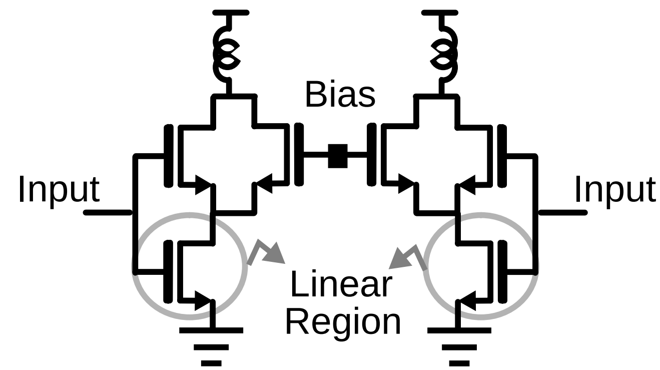
      60 dB linearity ➜ Input swing < 0.2 volt
  - Device output Characteristics:
    - High bias voltage for V_{DS} is desired.
    - With V_{DS} (bias) =2.3:

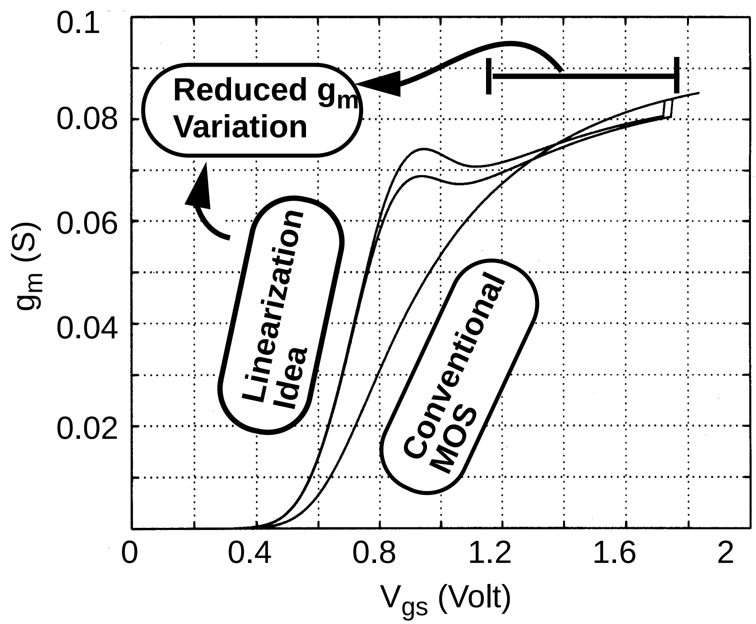
      60 dB linearity ➜ Output swing < 0.15 volt.
- **Output required swing:**

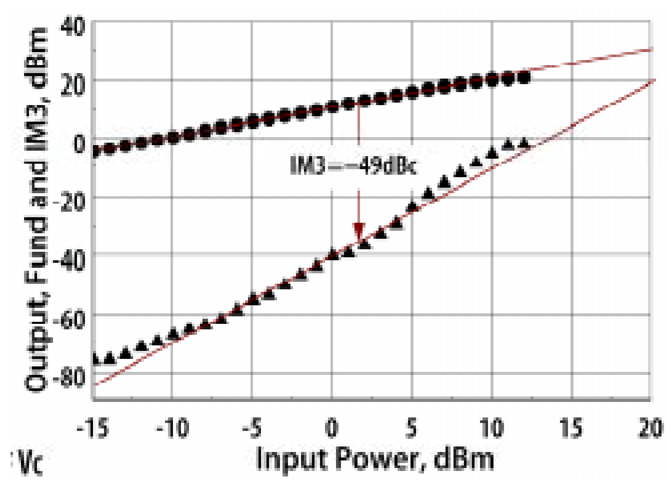
  Differential swing on the 50 ohm load = 1volt peak
- **Result :** *Cascode* stage is required to decrease the swing on the gain Transistor.

Power Amp Prototype: Distortion Cancellation

Third order nonlinearity of MOS in linear and saturation can cancel each other.

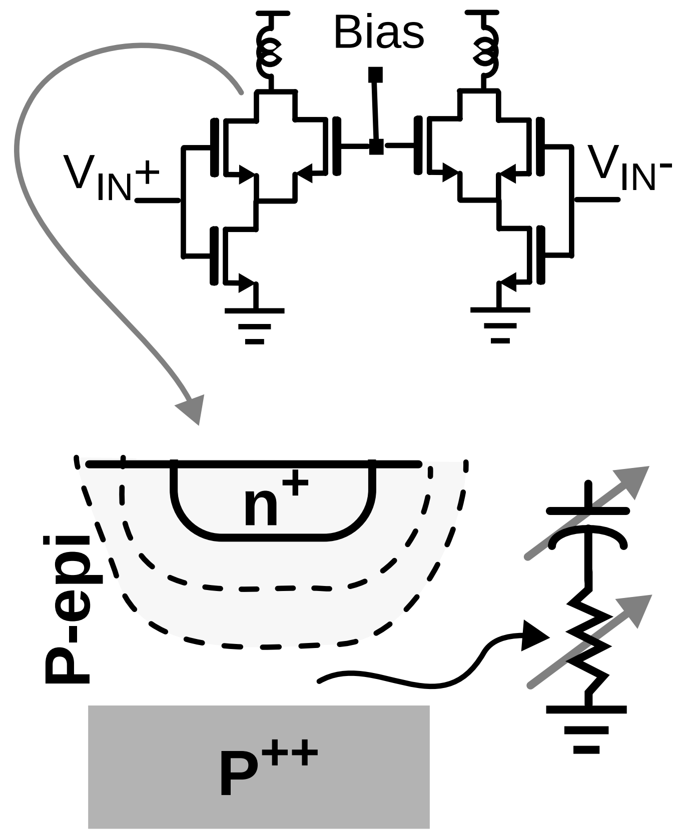






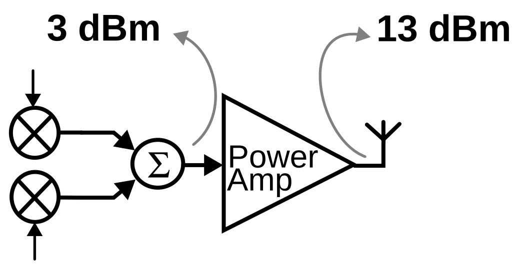
Preliminary Power Amp High Frequency Measurement Results

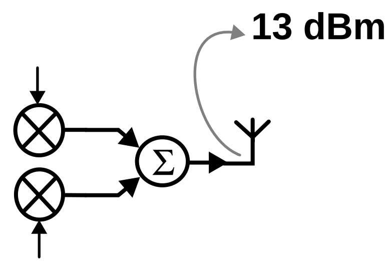
Frequency Gain		900 MHz 10 dB	2.4 GHz 6.1 dB	
IM3(dBc)	V_{DD} 3.3	43	30.5	32.5
$\eta(\%)$		4.7	5	5
IM3(dBc)	V_{DD} 4	50	30.5	33.8
$\eta(\%)$		3.2	4.1	4.2
IM3(dBc)	V_{DD} 5	50	33.2	38.5
$\eta(\%)$		3.2	3.2	3.2
		Output Power = 13 dBm		P_O= 11.5 dBm



Potential source of nonlinearity @ 2.4 GHz

Circuit Ideas
Power Mixer





Conventional Method

- Linearizing MOS by having small ac/DC current ➜

  large devices & low efficiency.
- Power-amp has large input capacitor.
- Small inductor for tuning the large capacitor produces small impedance.
- High current consumption in mixers

Alternative Method

- Using high-power mixers to generate 13 dBm required output power.
- Using feedback in the baseband of the mixer for linearization.
- Smaller devices can be used.

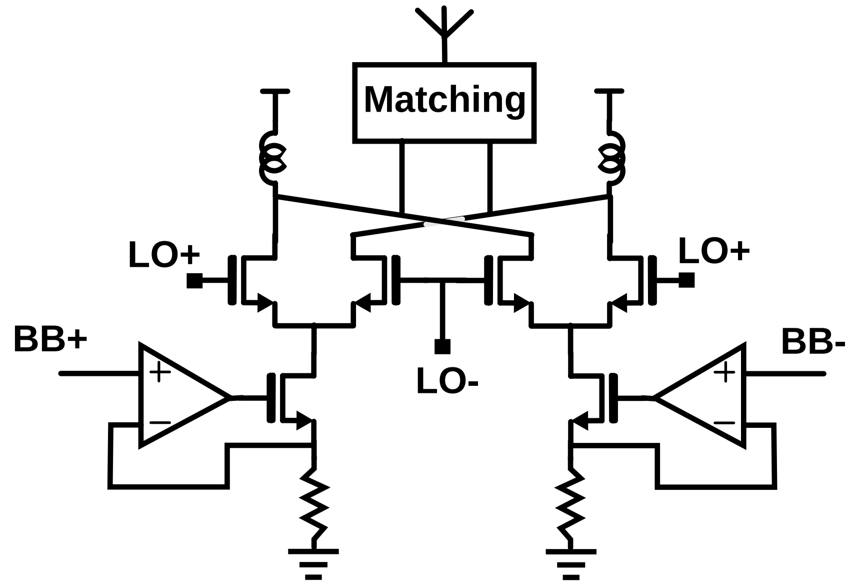
Power Mixer

Pros

- Linearity is achieved by baseband feed back.
- If the switching part is switched hard, it doesn't add to nonlinearity.
- Devices can be much smaller.
- Total power consumption may be lower.
- Feed back eliminates 2'nd harmonics of the baseband as well.

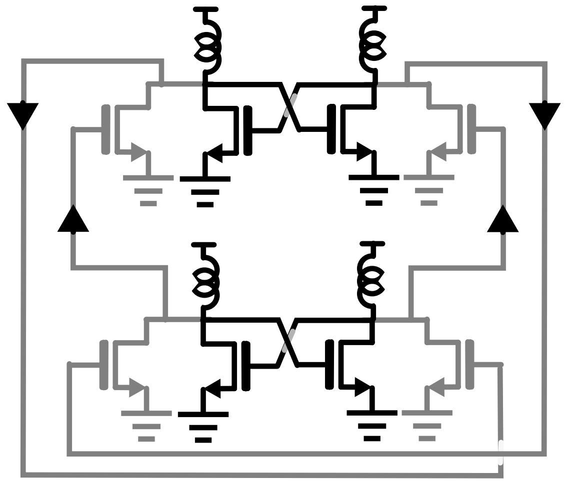
Cons

- 4 dB of mixing loss.
- Has larger device sizes.
- Requires higher LO power.
- Probably requires higher supply voltage.



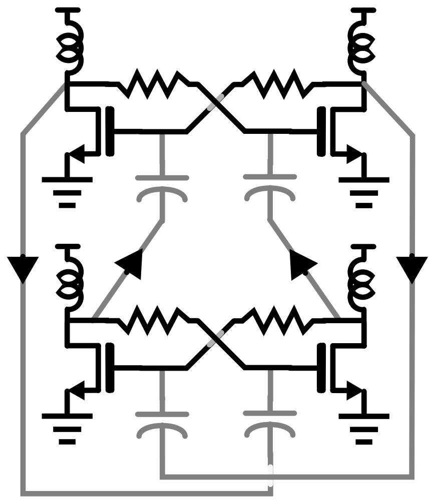
Max Baseband Frequency = 5 MHz

VCO idea



900 MHz project VCO

- Two LC oscillators, couple to each other.
- Phase noise limited by 1/f noise of the devices.
- Coupling through MOSs which consumes power and generates 1/f noise.

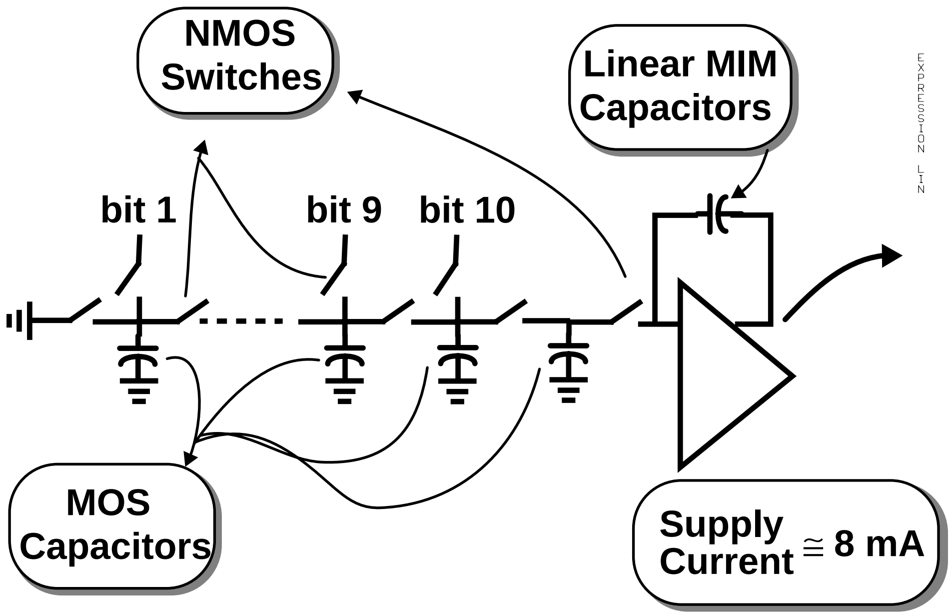


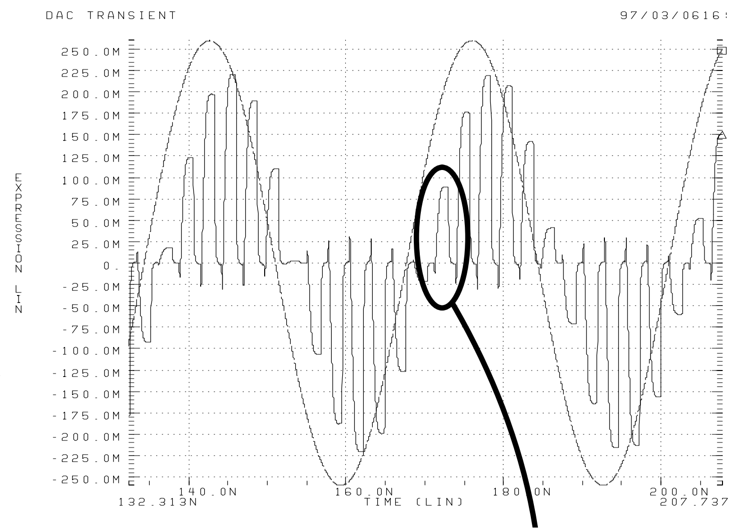
Idea for improvement

- Coupling through RC circuits.
- Coupling through resistors and capacitors (lower 1/f noise)
- Additional power consumption in core transistors (larger devices and higher g_m, lower noise)

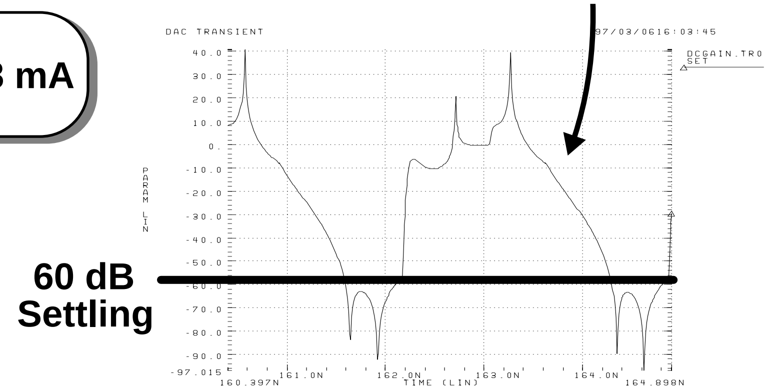
DAC for DDFS

10 bits, 300 MHz





360 MHz Sampling Frequency



Pure digital CMOS process

Second AGC

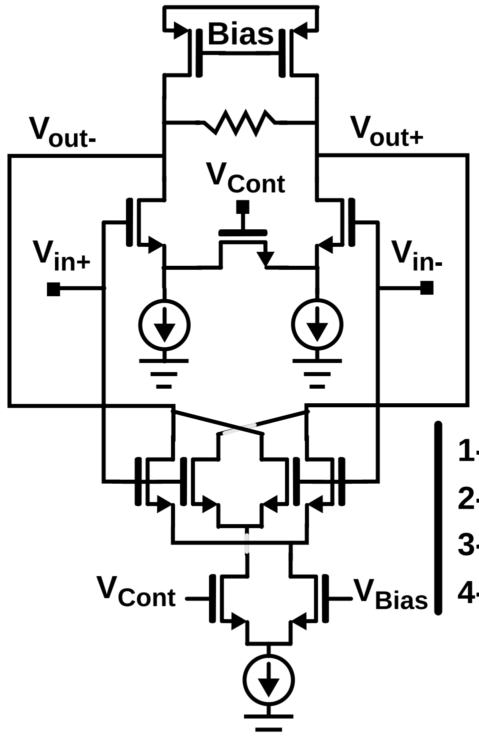
- 0 ~ 80 dB gain with 5 stages.
- Output power = 5 dBm.
- 90 dB gain ↔

  20 dB NF & 59 dB output linearity.
- 50 dB gain ↔

  45 dB output linearity.
- 0 dB gain ↔

  34 dB NF & 50 dB output linearity.
- High gain block turns off at low gain

  and low gain block turns off at high gain.
- Bias current: 6~12 mA



1- Large input signals
2- 0 < Gain < 6 dB
3- 1 mA bias current

1- Zero output @ large input
2- 0 < Gain < 16 dB
3- Low noise
4- 1.5 mA bias current

Impact & Achievements

- Demonstrate the capabilities of CMOS for 2.4 GHz band. Significant contribution to the definition of a new superior MOS model for industrial standard.
- Develope a highly linear, wide dynamic range, low noise CMOS transceiver:

  Tight specifications for building blocks demand innovative design leading to new techniques or significant improvements in the current techniques for each block.

- Achieve ultimate performance of the quadrature architecture.
- Highly integrated circuit. Minimum off-chip components. Highly reliable (fewer components for the whole system).