Harris Semiconductor

TechBrief

Harris Digital Signal Processing

QUADRATURE DOWN CONVERSION
WITH THE HSP45116, HSP43168 AND HSP43220

The Harris HSP45116 Numerically Controlled Oscillator/ Modulator (NCOM) can be combined with a low pass filter to perform down conversion on a digital signal. The NCOM rotates the spectrum of a real or complex signal and outputs a complex data stream. The signal of interest is now at base band, so that the output can be low pass filtered to eliminate unwanted signals (Figure 1).
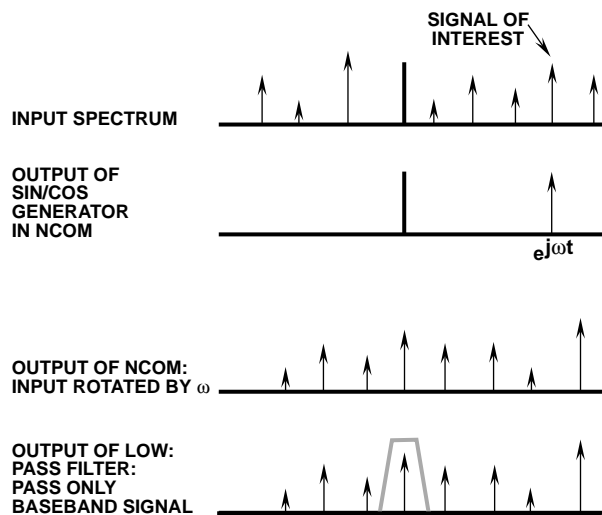

FIGURE 1. DOWN CONVERSION SPECTRAL PLOTS

If the spectrum of the signal of interest is sufficiently narrow, the output sample rate of the filter can be reduced to ease the throughput requirements of the downstream processing. Reducing the sample rate of a signal is commonly known as decimation. The input sample rate divided by the output sample rate is known as the decimation factor, or simply decimation. Note that decimation by one is equivalent to no decimation, and decimation by less than one is undefined. For the purposes of this discussion, base band signals will be divided into two categories: wide band signals, where the decimation factor is 16 or less, and narrow band signals, where the decimation is greater than 16.

Narrow Band Down Conversion

For narrow band output signals, Harris has a three chip set with a filter that is capable of decimation by up to 16,384. Figure 2 shows how the NCOM and HSP43220 Decimating Digital Filter (DDF) are connected to perform down conver-

sion and real to quadrature conversion of an input signal. This is a generalized block diagram which can be used as the basis for a specific design.

Several assumptions were made in defining this block diagram. Among these assumptions are:

- Input and output data are sixteen bits. Users requiring less than that should keep bit 15 as the most significant bit, grounding the unused bits on the input of the NCOM. In all cases, bits 0 through 15 on the output of the NCOM should be connected to the sixteen input bits of the DDF. To select the output bits of the DDF, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:

- Real Output: $\cos(An)\cos(Bn) = [\cos(An-Bn) + \cos(An+Bn)]$

- Imaginary Output: $\cos(An)\sin(Bn) = [\sin(An+Bn) - \sin(An-Bn)]$

- Note that the factor of $1/2$ has been omitted. The output of the Complex Multiplier is shifted left by one bit internally. For this reason, both the real and imaginary outputs have the same magnitude as the input.

- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD# signal is not exercised, so the initial phase of the NCOM is unknown.

- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.

- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.

- The filter clocks of the two DDFs are driven at a higher rate than the input data clocks. For many applications the FIR_CK, CK_IN and CLK signals can all be connected together. In this case the divide by N block is not needed.

- The DDFs are reset and started asynchronously with a pulse generator that receives asynchronous commands from an outside source and drives the two DDFs simultaneously. The DDF receiving the asynchronous start pulse performs the synchronization and starts the other part at the proper time.
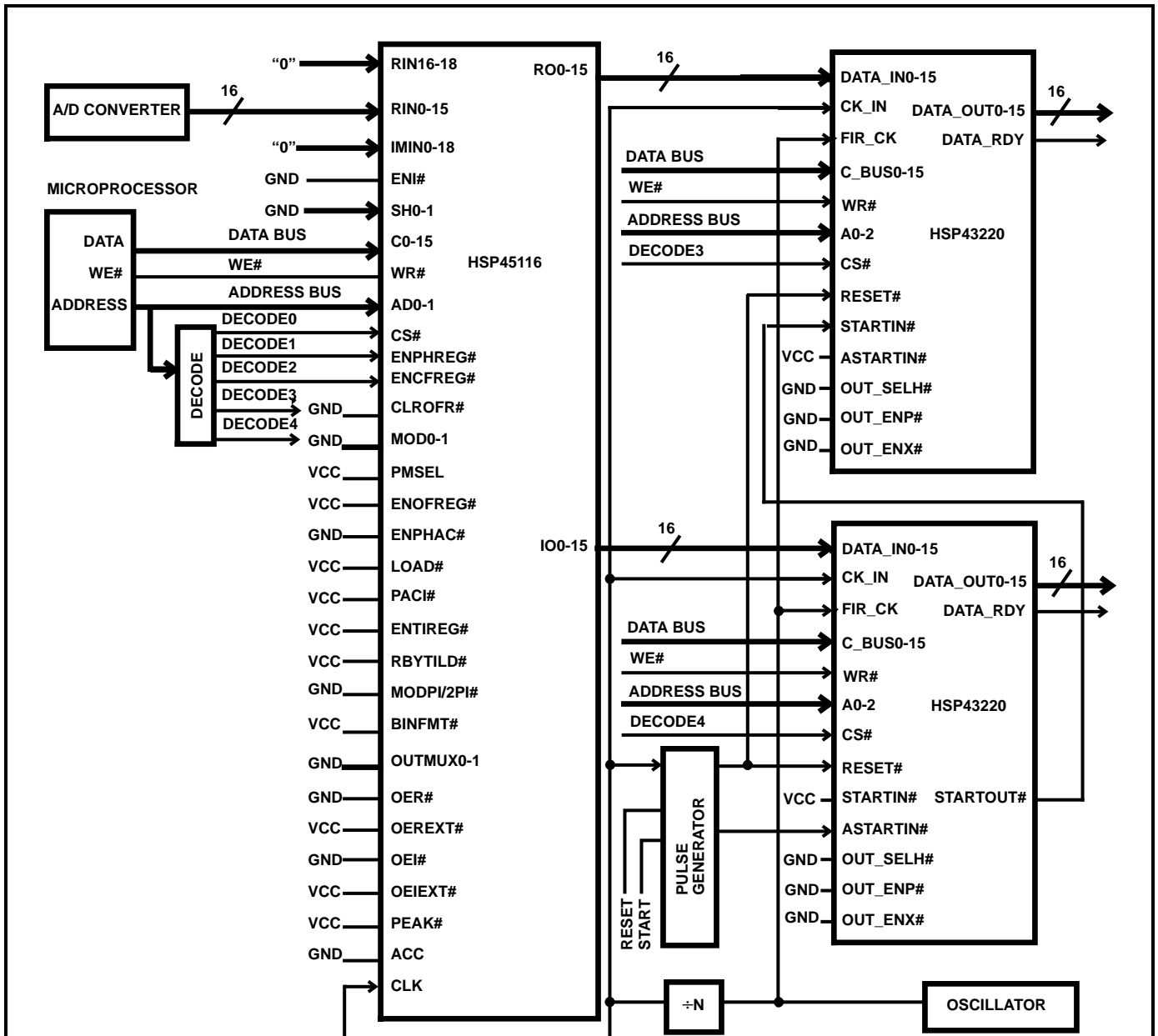
FIGURE 2. BLOCK DIAGRAM FOR QUADRATURE DOWN CONVERSION WITH HSP45116 AND HSP43220.
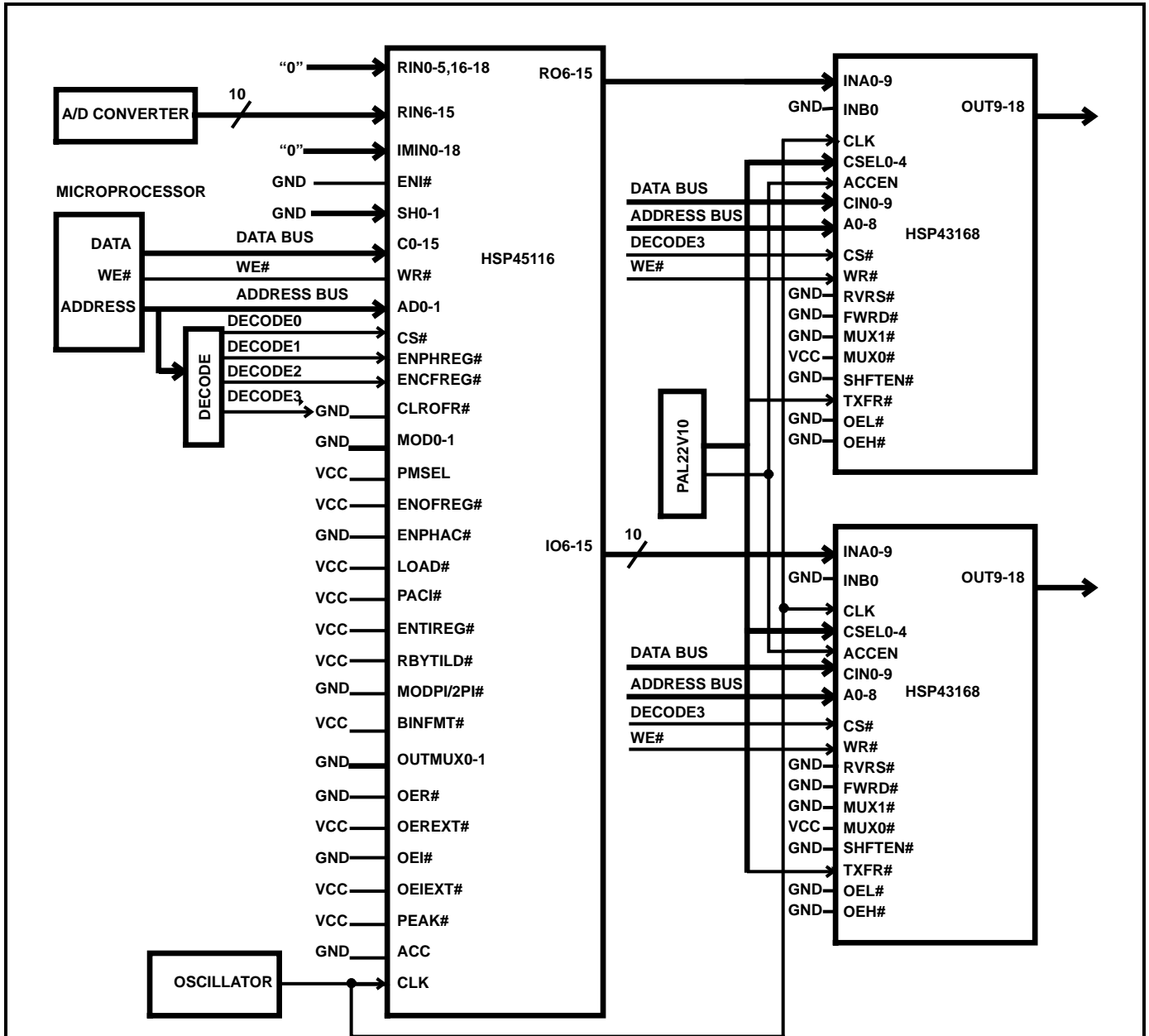
FIGURE 3. BLOCK DIAGRAM FOR WIDE BAND QUADRATURE DOWN CONVERSION WITH HSP45116 AND HSP43168.
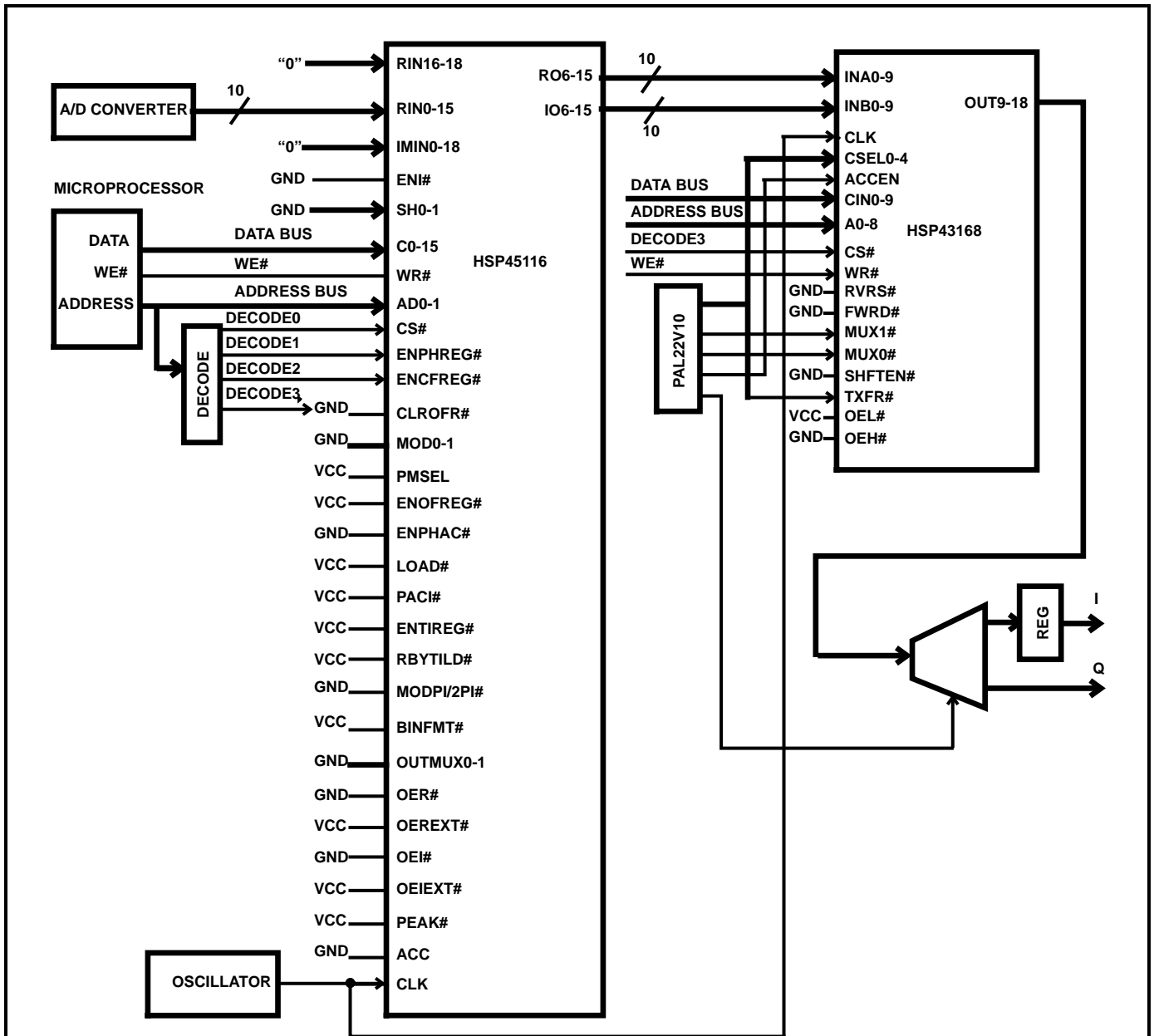
FIGURE 4. BLOCK DIAGRAM FOR WIDE BAND DOWN CONVERSION WITH HSP45116 AND HSP43168.

Wide Band Down Conversion

Figures 3 and 4 show how the NCOM and HSP43168 Dual FIR Filter (Dual FIR) are connected to perform down conversion and real to quadrature conversion of an input signal. Because the Dual FIR can implement either one or two filters, two block diagrams are shown. Figure 3 shows the case where each 43168 is implementing a single filter. The maximum number of coefficients in this case is 16 times the decimation factor for each filter. Figure 4 shows the same configuration with the exception that the Dual FIR is now configured as two independent filters, each with a maximum length of 8 times the decimation factor.

These are generalized block diagrams which can be used as the basis for a specific design. Note that they do not represent detailed schematics with all gates represented. For instance, the control signals are driven with a single PAL22V10 operating as a self contained state machine; it reality, the 22V10 may not have enough gates to generate all the necessary output sequences; in that case, it would be necessary to have a counter generate the states and use the PAL to decode the counter output, generate the control signals to the 43168, and reset the counter when the sequence is completed.

The design parameters of these circuits are:

- Input data is 10 bits. Users requiring less than that should keep bit 15 as the most significant bit of the NCOM, grounding the unused bits on the input. In all cases, bits 6 through 15 on the output of the NCOM should be connected to the input bits of the Dual. To select the output bits of the Dual, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:

- Real Output: $\cos(An)\cos(Bn) = [\cos(An-Bn) + \cos(An+Bn)]$

- Imaginary Output: $\cos(An)\sin(Bn) = [\sin(An+Bn) - \sin(An-Bn)]$

- Note that the factor of $^1/_2$ has been omitted. The output of the Complex Multiplier is shifted left by one bit internally. For this reason, both the real and imaginary outputs have the same magnitude as the input.

- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD# signal is not exercised, so the initial phase of the NCOM is unknown.

- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.

- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.

- The decimation rate in the Dual FIRs is greater than one. For no decimation, TXFR# should be grounded. Note that the maximum number of coefficients in the 43168 is eight or sixteen times the decimation rate, depending on the mode (see above).

Combined Narrow And Wide Band

In some applications, it is necessary to pass both wide and narrow band signals. In this case, both the HSP43220 and HSP43168 can be used in parallel, with the user selecting the output of either set of chips, depending on the characteristics of the signal of interest. Figure 5 shows this application, with most of the control signals eliminated for clarity. (These signals can be derived from the previous block diagrams.) In addition, note that the input data clock (CK_IN) and the FIR clock (FIR_CK) of the DDF have been connected together. This configuration is applicable when the input data rate is sufficiently high to allow the filter to operate at this rate also. If this is not the case, the divide by N circuit used in Figure 2 could be used, with the high speed clock driving the FIR_CK pins and the divided down clock used for all other clocks in the circuit.

New Products

Now available from Harris are the HSP50016 Digital Down Converter, which is a single chip quadrature down converter and low pass filter (Figure 6). In addition, the HSP43216 Half Band Filter allows the user to double the input sample rate of the NCOM for real signals (Figure 7). Contact your local Harris sales office or representative for more details on these and other new products from Harris.
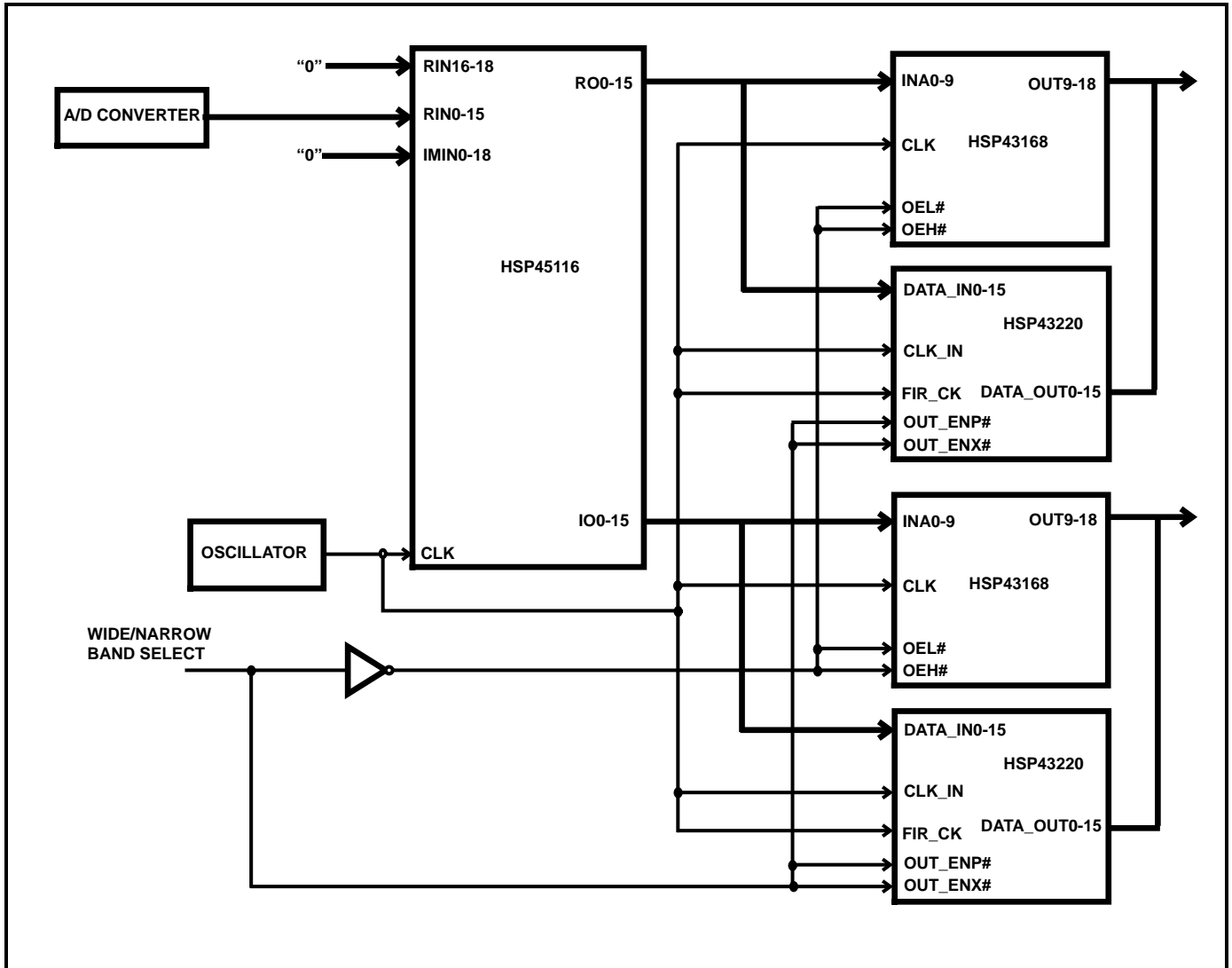
FIGURE 5. BLOCK DIAGRAM FOR QUADRATURE DOWN CONVERSION WITH HSP45116, HSP43220 AND HSP43168
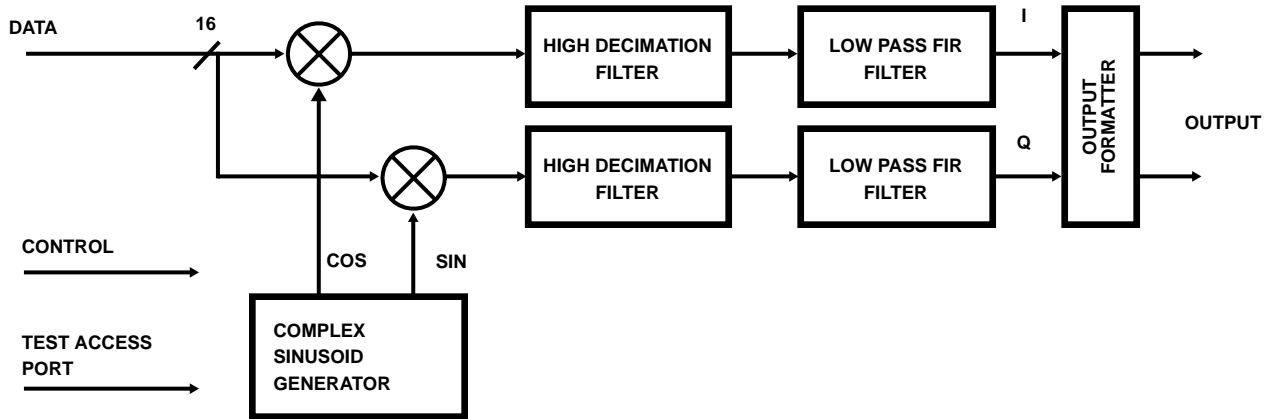
DATA 16

COS SIN

CONTROL

TEST ACCESS PORT

COMPLEX SINUSOID GENERATOR

HIGH DECIMATION FILTER

HIGH DECIMATION FILTER

LOW PASS FIR FILTER

LOW PASS FIR FILTER

I

Q

OUTPUT FORMATTER

OUTPUT

FIGURE 6. BLOCK DIAGRAM OF HSP50016 DIGITAL DOWN CONVERTER

52MHz REAL INPUT

26MHz COMPLEX SIGNAL

HSP43216

HSP45116

I

Q

HSP43220

HSP43220

BASEBAND SIGNAL

$\dfrac{\text{SAMPLE FREQ}}{2}$

$\dfrac{\text{SAMPLE FREQ}}{2}$

$\dfrac{\text{SAMPLE FREQ}}{2}$

$\dfrac{\text{SAMPLE FREQ}}{2}$

SIGNAL INPUT
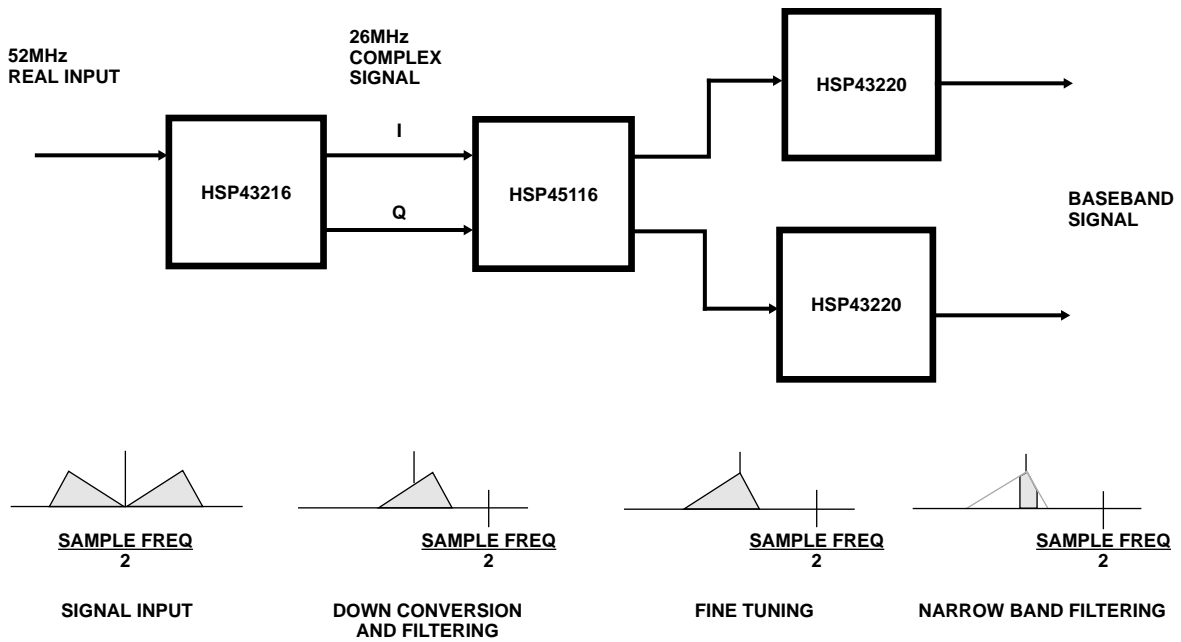
DOWN CONVERSION AND FILTERING

FINE TUNING

NARROW BAND FILTERING

FIGURE 7. HALF BAND FILTER IN QUADRATURE DOWN CONVERSION