Harris Semiconductor

APPNOTE

No. AN9616 August 1996

Harris Wireless

# Programming the HSP3824

Author: John Fakatselis

## Introduction


This application note serves as a firmware designers manual for the PRISM™ HSP3824 baseband processor. The note groups the programmable registers and their bit content by function. This note can serve as a quick reference for code development and system test and modification by function.

## SW Overview

The HSP3824 offers flexibility for various system configurations through its programmable features. Among other the user has many options to control synchronization time, link protocol formats, data rates, performance thresholds, and visibility to internal modem parameters and status.

### Preamble/Header

These configuration registers include preamble generation, transmit header modes and receive header modes. Preamble and header can be either generated internally from the HSP3824 or can be received from an external source i.e. a network processor.

### Modem Configuration

These configuration registers include configuration for transmitter and receiver modem. The transmit and receive symbol rates, scrambler configuration, PN code configuration and antenna selection are also programmed through these registers.

### I/O Configuration

These configuration registers include configuration of active signal levels (polarity) of HSP3824 I/O signals and set up of other miscellaneous I/O signal parameters. This is to provide flexibility and minimize glue logic to external circuits if there is a signal polarity issue.

### Test Port Configuration

These configuration registers include configuration for selection of internal HSP3824 signals and/or data to become available at the Test Port pins. These signals can be useful during debugging, regulatory compliance testing as well as to design enhanced external algorithms to improve overall radio performance.

### Threshold Settings

These configuration registers include a number of configurable threshold settings. They cover, Received Signal Strength Indication and Clear Channel Assessment threshold parameters, as well as, received signal quality thresholds used during acquisition and data tracking. By setting these acquisition and tracking thresholds, the user can define the desired modem performance i.e. set the probability of detection vs. the probability of false alarm ratio.

### A/D Calibration

These configuration registers include configuration data to activate the A/D level adjustment circuit of the HSP3824. This circuit is designed to maximize utilization of the A/D dynamic range. This programmable circuit tries to keep the A/Ds close to saturation.

### Modem Status

These configuration registers include information that represent both control and status registers (read-only). The status components indicate the real time state of the modem operation.

### Signal Status

These configuration registers include information that represent modem parameter (read-only) registers. These modem status components are updated real time. They can be used to design external SW or HW algorithms to improve overall modem performance. In addition this set of registers provide information on the link protocol (header) that is presently in use.

## Description of Configuration Register Assignments by Function.

The following paragraphs describe the configuration register (CR) content of the programmable HSP3824 registers. The bits within the CR that define the particular function or data are also indicated. The CR description and references below are broken by the primary HSP3824 programmable functional groups which are:

- Preamble/ header.
- Modem configuration
- I/O configuration
- Test Port configuration
- Threshold settings
- A/D calibration
- Modem status
- Signal status

This can serve as a quick reference to program or to modify registers by function. Refer also to the HSP3824 data sheet for description of the hardware algorithms at its appropriate sections. An example of a default set up is also attached to this note.

## Preamble/Header

**Preamble Generation CR3<2:2>**

This control bit is used to select the origination of the Preamble/Header information. The preamble and header can be either generated internally by the HSP3824 or from an external source.

**Transmit Mode CR0<4:3>**

These control bits are used to select one of the four Preamble Header modes for transmitting data. The four modes contain different combinations of fields.

CR0<4:3> Header Contents

00 SFD, field

01 SFD and CRC16, fields

10 SFD, Length and CRC16, fields

11 SFD, Signal, Length and CRC16, fields

**Receive Mode CR2<1:0>**

These control bits are used to select one of four Preamble Header modes for receiving data.

CR2<1:0> Header Contents

00 SFD

01 SFD and CRC16

10 SFD, Length and CRC16

11 SFD, Signal, Length and CRC16

**Transmit Preamble Length CR56<7:0>**

This control register defines the Preamble length field value.

**Start Frame Delimiter Definition CR49<7:0> CR50<7:0>**

These control registers contain the Start Frame Delimiter used for both the Transmit and Receive header. This field is the address field for each individual receiver within the network.

**Start Frame Delimiter Timer Enable CR0<2:2>**

This control bit is used to enable the Start Frame Delimiter timer. If the timer expires before the SFD has been detected, the HSP3824 returns to acquisition mode. The search time is defined by the start frame delimiter value registers.

**Start Frame Delimiter Value CR41<7:0>**

This control register contains the number of symbol periods for the demodulator to search for a SFD in a receive header before returning to acquisition mode.

**Data Field Counter Enable CR0<1:1>**

This control bit is used to enable/disable counting the number of data bits in the length field embedded in the header. The HSP3824 returns to acquisition mode at the end of the count as defined by the “Length” field of the header. This can only be used in header modes 2 and 3.

**CRC Check Enable CR2<5:5>**

This control bit is used to enable/disable the CRC16 check on the received Header.

## Modem Configuration

### TRANSMIT CONFIGURATION

**Chips per Symbol CR3<6:5>**

These control bits are used to select the number of chips per symbol used in the I and Q transmit paths.

| CR3<6:5> | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Chips/Symbol | 11 | 13 | 15 | 16 |

**Rate Divisor CR3<4:3>**

These control bits are used to select the divide ratio required to achieve the required data rate (refer to the HSP3824 data sheet).

| CR3<4:3> | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Divisor | 2 | 4 | 8 | 16 |

**Antenna Select CR0<7:7>**

This control bit is used to select the transmit antenna (half-duplex mode only).

**Modulation CR3<1:1>**

This control bit is used to select the signal modulation type for the transmit packet.

**Spread Sequence CR13<7:0> CR14<7:0>**

These control registers contain the spreading code for the I and Q transmit paths.

## RECEIVE CONFIGURATION

**Chips per Symbol CR2<7:6>**

These control bits are used to select the number of chips per symbol used in the I and Q receive paths.

| CR2<7:6> | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Chips/Symbol | 11 | 13 | 15 | 16 |

**Rate Divisor CR2<4:3>**

These control bits are used to select the divide ratio required for the desired receive data rate.

| CR2<4:3> | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Divisor | 2 | 4 | 8 | 16 |

**Antenna Select CR0<6:6>**

This control bit is used to select the receive antenna (single antenna mode only).

**Modulation CR3<0:0>**

This control bit is used to select the signal modulation type for the receive packet.

**Spread Sequence CR20<7:0> CR21<7:0>**

These control registers contain the despreading code for the I and Q receive paths.

**Scrambler Taps CR16<6:0>**

This control register contains the tap configuration for the transmit scrambler / receive descrambler.

**Scrambler Seed CR15<6:0>**

This control register contains the seed value for the transmit scrambler / receive descrambler.

**Antenna Operation CR0<5:5>**

This control bit is used to select between full duplex and half duplex operation.

**Antenna Mode CR2<2:2>**

This control bit is used to select single or dual antenna mode.

## *I/O Configuration*

**Allow Microprocessor Rate Change CR1<7:7>**

This control bit is used to enable/disable constant data rates to the external processor that receives the demodulated data from the HSP3824. Rate changes from DBPSK to DQPSK within the same packet can be programmed to be transparent to the external processor.

**Invert Transmit Clock Phase CR9<0:0>**

This control bit is used to select the phase of the transmit output clock.

**Assert TX_RDY Clock Count CR1<6:2>**

These control bits are used to define the number of clocks before the first data bit that TX_RDY will be asserted.

## ACTIVE SIGNAL LEVELS

These components allow the user to invert the sense of certain signals available as pins on the HSP3824.

**MAC Data Ready (MD_RDY) CR9<6:6>**

This control bit is used to select the active level of the MD_RDY signal.

**Clear Channel Assessment (CCA) CR9<5:5>**

This control bit is used to select the active level of the CCA signal.

**Energy Detect (ED) CR9<4:4>**

This control bit is used to select the active level of the ED signal.

**Carrier Sense (CRS) CR9<3:3>**

This control bit is used to select the active level of the CRS signal.

**Transmit Data Ready (TX_RDY) CR9<2:2>**

This control bit is used to select the active level of the TX_RDY signal.

**Transmit Power Enable (TX_PE) CR9<1:1>**

This control bit is used to select the active level of the TX_PE signal.

## *Test Port Configuration*

**Test Mode CR4<7:0>**

The HSP3824 provides the capability to access a number of internal signals and/or data through the test port pins TEST 0-7 and TEST_CLK. The TEST_CLK is selected given the data that is clocked out from TEST 0-7 port. TX_CLK is intended to be used to clock the TEST 0-7 data from the HSP3824.

**(0) Normal Operation Mode**

<7:7> Carrier Sense (CRS)

<6:6> Energy Detect (ED)

<5:3> Reserved

<2:2> Initial Detect

<1:0> Reserved

TEST_CLK Internal TX Clock (TX chip rate)

**(1) Correlator Test Mode**

<7:0> Correlator Magnitude (PN correlator)

TEST_CLK Internal TX Clock (TX chip rate)

**(2) Frequency Test Mode**

<7:0> Frequency offset Register

TEST_CLK Subsample Clock (Rx symbol rate)

**(3) Phase Test Mode**

<7:0> Phase (instantenous I,Q)

TEST_CLK Subsample Clock (Rx symbol rate)

**(4) NCO Test Mode**

<7:0> Phase Accum Register (8 most significant bits)

TEST_CLK Subsample Clock (Rx symbol rate)

**(5) SQ Test Mode**

<7:0> Signal Quality (SQ) Phase Variance (8 most significant bits)

TEST_CLK Load Signal Quality Signal

**(6) Bit Sync Test Mode 1**

<7:0> Bit Sync Accum

TEST_CLK Internal RX Clock

**(7) Bit Sync Test Mode 2**

<7:0> SQ Bit Sync Reference Data (8 most significant bits)

TEST_CLK Load SQ Signal

**(8) A/D Cal Test Mode**

<7:7> Carrier Sense (CRS)

<6:6> Energy Detect (ED)

<5:5> Reserved

<4:0> A/D Calibrate

TEST_CLK (Internal RX Clock)

## Threshold Settings

**Received Signal Strength Indication (RSSI) CR19<5:0>**

These control bits are used to specify the RSSI threshold for measuring and generating the energy detect (ED) signal. When RSSI exceeds this threshold, ED is declared.

**Clear Channel Assessment Timer CR17<7:0>**

This control register is used to configure the period of the time-out threshold of the CCA watchdog timer.

**Clear Channel Assessment Cycle CR18<7:0>**

This control register is used to configure how many times the CCA timer is allowed to reach its maximum count before it declares that the channel is clear (independent of the actual energy measured in the channel).

**Enable 1/4 Chip Adjust During Acquisition/Data CR5<6:6>**

This control bit is used to enable/disable 1/4 chip timing adjustments during acquisition or data. The default is 1/2 chip adjustments.

**Receive Bit Synch Amplitude (Acquisition/Data) CR22<7:0> CR23<7:0>**

These control registers are used to specify the bit synch amplitude quality threshold used for acquisition and for data. See typical values in the HSP3824 data sheet.The received signal must be above this programmable value to be declared valid.

**Receive Phase Variance (Acquisition/Data) CR30<7:0> CR31<7:0>**

These control registers are used to specify the phase variance quality threshold used for acquisition and for data. See typical values in the HSP3824 data sheet. The received signals phase variance has to be less than this programmable value to be declared as valid signal.

## A/D Calibration

**Reference Value CR1<1:1>**

This control bit is used to select whether internal A/D calibration circuit is active or not and if not, sets the reference to mid-scale.

**Last Value CR1<0:0>**

This control bit is used to select whether internal A/D calibration circuit is held at its most recent value.

**Positive Increment Adjust CR11<7:0>**

This control register contains the value used for positive increments of the level adjusting circuit of the A/D reference. These positive increment steps define how fast the A/D will be driven to saturation.

**Negative Increment Adjust CR12<7:0>**

This control register contains the value used for negative increments of the level-adjusting circuit of the A/D reference. These negative increments define the back off step size from when the A/D reaches saturation.

## Modem Status

**Transmit Ready (TX_RDY) CR7<7:7>**

This status bit indicates the status of the TX_RDY output pin. It is only used when the Preamble/Header is generated internally within the HSP3824.

**Antenna CR7<6:6>**

This status bit indicates the antenna selected by the device (status of the ANTSEL pin) during antenna diversity.

**Clear Channel Assessment (CCA) CR7<5:5>**

This status bit indicates the status of the Clear Channel Assessment output pin.

**Carrier Sense (CRS) CR7<4:4>**

This status bit indicates the status of Carrier Sense (or PN lock).

**RSSI vs. Threshold CR7<3:3>**

This status bit indicates whether the RSSI signal is above or below threshold (or energy detect (ED)).

**MAC Data Ready (MD_RDY) CR7<2:2>**

This status bit indicates the status of the MD_RDY output pin. It signals that a valid Preamble/Header has been received and that the next available bit on the RXD bus will be the first data packet bit.

**Transmit Power Enable (TX_PE) CR7<1:1>**

This status bit indicates whether the external device has acknowledged that the channel is clear for transmission (or status of the TX_PE pin).

**Valid CRC16 CR7<0:0>**

This status bit indicates whether a valid CRC16 has been calculated for the Header information. The CRC16 does not cover the preamble bits or the data packet.

**Packet Status CR8<7:7>**

This status bit indicates whether a valid packet has been received. This is meaningful only when the device operates under the full protocol (mode 3).

**Start Frame Delimiter Search Timer CR8<6:6>**

This status bit indicates the status of the SFD search timer.

**Modulation Type CR8<5:5>**

This status bit indicates the modulation type for the data packet. Preamble and Header data are always at 1MBPS.

## *Signal Status*

### TRANSMIT PREAMBLE INFORMATION

**Service Field CR51<7:0>**

This control register contains the value of the service field to be transmitted in a Header.

**Length Field CR52<7:0> CR53<7:0>**

These control registers contain the value of the length field to be transmitted. It indicates the number of bits transmitted in the data packet.

**CRC16 Field CR54<7:0> CR55<7:0>**

These status registers indicate the calculated CRC16 for the transmitted header.

### RECEIVE PREAMBLE INFORMATION

**Service Field CR44<7:0>**

This status register contains the value of the service field received in a Header.

**Length Field CR45<7:0> CR46<7:0>**

These status registers contain the value of the length field of the received packet. It indicates the number of bits transmitted in the data packet.

**CRC16 Field CR47<7:0> CR48<7:0>**

These status registers indicate the received CRC16 for the received header.

### SIGNAL FIELD

**BPSK CR42<7:0>**

This control register contains the 8-bit value indicating that the data packet modulation is DBPSK.

**QPSK CR43<7:0>**

This control register contains the 8-bit value indicating that the data packet modulation is DQPSK.

### RECEIVE SIGNAL QUALITY INDICATORS

**Bit Synch Amplitude Acquisition CR24<6:0> CR25<7:0>**

These status registers contain the measured bit synch amplitude signal quality during acquisition.

**Bit Synch Amplitude Data CR28<6:0> CR29<7:0>**

These status registers contain the measured bit synch amplitude signal quality during data tracking.

**Phase Variance Acquisition CR32<7:0> CR33<7:0>**

These status registers contain the measured phase variance signal quality during acquisition.

**Phase Variance Data CR36<7:0> CR37<7:0>**

These status registers contain the measured phase variance signal quality during data tracking.

**RSSI Value CR10<5:0>**

These status bits contain the value of the RSSI analog input signal from the on-chip ADC. This register is updated at the chip rate divided by 11.

**Receive Signal Quality for Best Antenna Dwell CR38<7:0>**

This status register contains the bit synch amplitude signal quality measurement derived from the Bit Synch signal quality stored in the CR28-29 registers of the HSP3824. This value is the result of the signal quality measurement for the best antenna dwell in the antenna diversity mode.

**DEFAULT CONFIGURATION**

Table 1 contains a set of default configuration values that can be used for QPSK and BPJK modulation. These values can be initially used for systems test and then modified as appropriate, per each application. The default configuration table is followed by the detail description of all the available registers of the HSP3824.

**TABLE 1. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION**

| REGISTER | NAME | TYPE | REG ADDR IN HEX | QPSK | BPSK |
|---|---|---|---|---|---|
| CR0 | MODEM CONFIG. REG A | R/W | 00 | 3C | 64 |
| CR1 | MODEM CONFIG. REG B | R/W | 04 | 00 | 00 |
| CR2 | MODEM CONFIG. REG C | R/W | 08 | 07 | 24 |
| CR3 | MODEM CONFIG. REG D | R/W | 0C | 04 | 07 |
| CR4 | INTERNAL TEST REGISTER A | R/W | 10 | 00 | 00 |
| CR5 | INTERNAL TEST REGISTER B | R/W | 14 | 00 | 00 |
| CR6 | INTERNAL TEST REGISTER C | R | 18 | X | X |
| CR7 | MODEM STATUS REGISTER A | R | 1C | X | X |
| CR8 | MODEM STATUS REGISTER B | R | 20 | X | X |
| CR9 | I/O DEFINITION REGISTER | R/W | 24 | 00 | 00 |
| CR10 | RSSI VALUESTATUS REGISTER | R | 28 | X | X |
| CR11 | ADC_CAL_POS REGISTER | R/W | 2C | 01 | 01 |
| CR12 | ADC_CAL_NEG REGISTER | R/W | 30 | FD | FD |
| CR13 | TX_SPREAD SEQUENCE(HIGH) | R/W | 34 | 05 | 05 |
| CR14 | TX_SPREAD SEQUENCE (LOW) | R/W | 38 | B8 | B8 |
| CR15 | SCRAMBLE_SEED | R/W | 3C | 7F | 7F |
| CR16 | SCRAMBLE_TAP (RX AND TX) | R/W | 40 | 48 | 48 |
| CR17 | CCA_TIMER_TH | R/W | 44 | 2C | 2C |
| CR18 | CCA_CYCLE_TH | R/W | 48 | 03 | 03 |
| CR19 | RSSI_TH | R/W | 4C | 1E | 1E |
| CR20 | RX_SPREAD SEQUENCE (HIGH) | R/W | 50 | 05 | 05 |
| CR21 | RX_SREAD SEQUENCE (LOW) | R/W | 54 | B8 | B8 |
| CR22 | RX_SQ1_ IN_ACQ (HIGH) THRESHOLD | R/W | 58 | 01 | 01 |
| CR23 | RX-SQ1_ IN_ACQ (LOW) THRESHOLD | R/W | 5C | E8 | E8 |
| CR24 | RX-SQ1_ OUT_ACQ (HIGH) READ | R | 60 | X | X |
| CR25 | RX-SQ1_ OUT_ACQ (LOW) READ | R | 64 | X | X |
| CR26 | RX-SQ1_ IN_DATA (HIGH) THRESHOLD | R/W | 68 | 0F | 0F |
| CR27 | RX-SQ1-SQ1_ IN_DATA (LOW) THRESHOLD | R/W | 6C | FF | FF |
| CR28 | RX-SQ1_ OUT_DATA (HIGH)READ | R | 70 | X | X |
| CR29 | RX-SQ1_ OUT_DATA (LOW) READ | R | 74 | X | X |
| CR30 | RX-SQ2_ IN_ACQ (HIGH) THRESHOLD | R/W | 78 | 00 | 00 |

**TABLE 1. CONTROL REGISTER VALUES FOR SINGLE ANTENNA ACQUISITION (Continued)**

| REGISTER | NAME | TYPE | REG ADDR IN HEX | QPSK | BPSK |
|---|---|---|---|---|---|
| CR31 | RX-SQ2- IN-ACQ (LOW) THRESHOLD | R/W | 7C | CA | CA |
| CR32 | RX-SQ2_ OUT_ACQ (HIGH) READ | R | 80 | X | X |
| CR33 | RX-SQ2_ OUT_ACQ (LOW) READ | R | 84 | X | X |
| CR34 | RX-SQ2_IN_DATA (HIGH)THRESHOLD | R/W | 88 | 09 | 09 |
| CR35 | RX-SQ2_ IN_DATA (LOW) THRESHOLD | R/W | 8C | 80 | 80 |
| CR36 | RX-SQ2_ OUT_DATA (HIGH) READ | R | 90 | X | X |
| CR37 | RX-SQ2_ OUT_DATA (LOW) READ | R | 94 | X | X |
| CR38 | RX_SQ_READ; FULL PROTOCOL | R | 98 | X | X |
| CR39 | RESERVED | W | 9C | 00 | 00 |
| CR40 | RESERVED | W | A0 | 00 | 00 |
| CR41 | UW_Time Out_LENGTH | R/W | A4 | 90 | 90 |
| CR42 | SIG_DBPSK Field | R/W | A8 | 0A | 0A |
| CR43 | SIG_DQPSK Field | R/W | AC | 14 | 14 |
| CR44 | RX_SER_Field | R | B0 | X | X |
| CR45 | RX_LEN Field (HIGH) | R | B4 | X | X |
| CR46 | RX_LEN Field (LOW) | R | B8 | X | X |
| CR47 | RX_CRC16 (HIGH) | R | BC | X | X |
| CR48 | RX_CRC16 (LOW) | R | C0 | X | X |
| CR49 | UW -(HIGH) | R/W | C4 | F3 | F3 |
| CR50 | UW _(LOW) | R/W | C8 | A0 | A0 |
| CR51 | TX_SER_F | R/W | CC | 00 | 00 |
| CR52 | TX_LEN (HIGH) | R/W | D0 | FF | FF |
| CR53 | TX_LEN(LOW) | R/W | D4 | FF | FF |
| CR54 | TX_CRC16 (HIGH) | R | D8 | X | X |
| CR55 | TX_CRC16 (LOW) | R | DC | X | X |
| CR56 | TX_PREM_LEN | R/W | E0 | 80 | 80 |

## Control Registers, Address and Bit Location Specification

The following tables describe the function of each control register along with the associated bits in each control register.

**CONFIGURATION REGISTER 0 ADDRESS (0h) MODEM CONFIGURATION REGISTER A**

| | |
|---|---|
| Bit 7 | This bit selects the transmit antenna, controlling the output ANT_SEL pin. It is only used in half duplex mode. (Bit 5 = 0)<br>Logic 1 = Antenna A.<br>Logic 0 = Antenna B. |
| Bit 6 | In single antenna operation this bit is used as the output of the ANT_SEL pin. In dual antenna mode this bit is ignored.<br>Logic 1 = Antenna A.<br>Logic 0 = Antenna B. |
| Bit 5 | This control bit is used to select between full duplex and half duplex operation. If set for full duplex operation, the ANT_SEL pin reflects the setting of CR0 bit 7 when TX_PE is active and reflects the receiver's choice when TX_PE is inactive. In full duplex operation, the ANT_SEL pin always reflects the receiver's choice antenna.<br>Logic 1 = full duplex.<br>Logic 0 = half duplex. |
| Bit 4, 3 | These control bits are used to select one of the four input Preamble Header modes for transmitting data. The preamble and header are DBPSK for all modes of operation. Mode 0 is followed by DBPSK data. For modes 1-3, the data can be configured as either DBPSK or DQPSK. This is a "don't care" if the header is generated externally. |

| MODE | BIT 4 | BIT 3 | MODE DESCRIPTION |
|---|---|---|---|
| 0 | 0 | 0 | Preamble with SFD Field. |
| 1 | 0 | 1 | Preamble with SFD, and CRC16. |
| 2 | 1 | 0 | Preamble with SFD, Length, and CRC16. |
| 3 | 1 | 1 | Full preamble and header. |

| | |
|---|---|
| Bit 2 | This control bit is used to enable the SFD (Start Frame Delimiter) timer. If the time is set and expires before the SFD has been detected, the HSP3824 will return to its acquisition mode.<br>Logic 1: Enables the SFD timer to start counting once the PN acquisition has been achieved.<br>Logic 0: Disables the SFD Timer. |
| Bit 1 | This control bit enables counting the number of data bits per the length field embedded in the header. Only used in header modes 2 and 3. Then according to the count it returns the processor into its acquisition mode at the end of the count. If length field is 0000h, modem will reset at end of SFD regardless of this bit setting.<br>Logic 1 = Enable Length Time Out.<br>Logic 0 = Disabled. |
| Bit 0 | Unused don't care. |

**CONFIGURATION REGISTER 1 ADDRESS (04h) MODEM CONFIGURATION REGISTER B**

| | |
|---|---|
| Bit 7 | When active this bit maintains the RXCLK and TXLK rates constant for preamble and data transfers even if the data is modulated in DQPSK. This bit is used if the external processor can not accommodate rate changes. This is an active high signal. The rate used is the QPSK rate and the BPSK header bits are double clocked. |
| Bit 6, 5, 4, 3, 2 | These control bits are used to define a binary count (N) from 0 - 31. This count is used to assert TX_RDY N - clocks (TXCLK) before the beginning of the first data bit. If this is set to zero, then the TX_RDY will be asserted immediately after the last bit of the Preamble Header. |
| Bit 1 | When active the internal A/D calibration circuit sets the reference to mid-scale. When inactive then the calibration circuit adjusts the reference voltage in real time to optimize I, Q levels.<br>Logic 1 = Reference set at mid-scale (fixed).<br>Logic 0 = Real time reference adjustment. |
| Bit 0 | When active the A/D calibration circuit is held at its last value.<br>Logic 1 = Reference held at the most recent value.<br>Logic 0 = Real time reference level adjustment. |

**CONFIGURATION REGISTER 2 ADDRESS (08h) MODEM CONFIGURATION REGISTER C**

**Bit 7, 6**

These control bits are used to select the number of chips per symbol used in the I and Q paths of the receiver matched filter correlators (see table below).

| CHIPS PER SYMBOL | BIT 7 | BIT 6 |
|---|---|---|
| 11 | 0 | 0 |
| 13 | 0 | 1 |
| 15 | 1 | 0 |
| 16 | 1 | 1 |

**Bit 5**

This control bit is used to disable the CRC16 check. When this bit is set, the processor will accept the received packet and any packet error checks have to be detected externally. The HSP3824 will remain in the receive mode until either the carrier is lost or the network processor resets the device to the acquisition mode, or if, in modes 2 or 3, the length times out.
Logic 1 = Disable receiver error checks.
Logic 0 = Enable receiver checks.

**Bit 4, 3**

These control bits are used to select the divide ratio for the demodulators receive chip clock timing.The value of N is determined by the following equation:
Symbol Rate = MCLK/(N x Chips per symbol).

| MASTER CLOCK/N | BIT 4 | BIT 3 |
|---|---|---|
| N = 2 | 0 | 0 |
| N = 4 | 0 | 1 |
| N = 8 | 1 | 0 |
| N = 16 | 1 | 1 |

**Bit 2**

This control bit sets the receiver into single or dual antenna mode. The Preamble acquisition processing length and whether the modem scans antennas is controlled by this bit. If in single antenna mode, the ANT_SEL pin reflects CR0 bit 6 otherwise it reflects the receiver's choice of antenna.
Logic 0 = Acquisition processing is for dual antenna acquisition.
Logic 1 = Acquisition processing is for single antenna acquisition.

**Bit 1, 0**

These control bits are used to indicate one of the four Preamble Header modes for receiving data. Each of the modes includes different combinations of Header fields. Users can choose the mode with the fields that are more appropriate for their networking requirements. The Header fields that are combined to form the various modes are:

- SFD field
- CRC16 field
- Data length field (indicates the number of data bits that follow the Header information)
- Full protocol Header

| INPUT MODE | BIT 1 | BIT 0 | RECEIVE PREAMBLE - HEADER FIELDS |
|---|---|---|---|
| 0 | 0 | 0 | Preamble, with SFD Field |
| 1 | 0 | 1 | Preamble, with SFD, CRC16 |
| 2 | 1 | 0 | Preamble, with SFD Length, CRC16 |
| 3 | 1 | 1 | Preamble, with Full Protocol Header |

**CONFIGURATION REGISTER 3 ADDRESS (0Ch) MODEM CONFIGURATION REGISTER D**

| | |
|---|---|
| Bit 7 | Reserved (must set to “0”). |
| Bit 6, 5 | These control bits combined are used to select the number of chips per symbol used in the I and Q transmit paths (see table below).<br><br>**CHIPS PER / BIT 6 / BIT 5**<br>11 / 0 / 0<br>13 / 0 / 1<br>15 / 1 / 0<br>16 / 1 / 1 |
| Bit 4, 3 | These control bits are used to select the divide ratio for the transmit chip clock timing.<br>NOTE: The value of N is determined by the following equation: Symbol Rate = MCLK/(N x Chips per symbol)<br><br>**MASTER / BIT 4 / BIT 3**<br>N = 2 / 0 / 0<br>N = 4 / 0 / 1<br>N = 8 / 1 / 0<br>N = 16 / 1 / 1 |
| Bit 2 | This control bit is used to select the origination of Preamble/Header information.<br>Logic 1: The HSP3824 generates the Preamble and Header internally by formatting the programmed header information and generating a TX_RDY to indicate the beginning of the data packet.<br>Logic 0: Accepts the Preamble/Header information from an externally generated source. |
| Bit 1 | This control bit is used to indicate the signal modulation type for the transmitted data packet. When configured for mode 0 header, or mode 3 and external header, this bit is ignored. See Register 0 bits 4 and 3.<br>Logic 1 = DBPSK modulation for data packet.<br>Logic 0 = DQPSK modulation for data packet. |
| Bit 0 | This control bit is used to indicate the signal modulation type for the received data packet Used only with header modes 1 and 2. See register 2-bits 1 and 0.<br>Logic 1 = DBPSK.<br>Logic 0 = DQPSK. |

**CONFIGURATION REGISTER 4 ADDRESS (10h) INTERNAL TEST REGISTER A**

| | |
|---|---|
| Bit 7 - 0 | These control bits are used to direct various internal signals to test port output pins. These internal signals are monitored to fault isolate the device at manufacturing testing. During normal operation, the value 0h is recommended. This will result to the following signals becoming available at the output test pins of the device:<br>Pin 46 (TEST7): Carrier Sense (CRS), a Logic 1 indicates PN lock.<br>Pin 45 (TEST6): Energy Detect (ED), a Logic 1 indicates that there is energy detected in the channel. The ED goes active when the RSSI exceeds the threshold level programmed by the user.<br>Pin 1 (TEST_CK): PN clock. |

**CONFIGURATION REGISTER 5 ADDRESS (14h,18h) INTERNAL TEST REGISTER B**

| | |
|---|---|
| Bits 7 - 0 | These bits need to be programmed to 0h. They are used for manufacturing test only. |

**CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A**

| | |
|---|---|
| Bit 7 | This bit indicates the status of the TX_RDY output pin. TX_RDY is used only when the HSP3824 generates the Preamble/Header data internally.<br>Logic 1: Indicates that the HSP3824 has completed transmitting Preamble header information and is ready to accept data from the external source (i.e. MAC) to transmit.<br>Logic 0: Indicates that the HSP3824 is in the process of transmitting Preamble Header information. |
| Bit 6 | This status bit indicates the antenna selected by the device.<br>Logic 0: Antenna A is selected.<br>Logic 1: Antenna B is selected. |

**CONFIGURATION REGISTER 7 ADDRESS (1Ch) MODEM STATUS REGISTER A (Continued)**

| | |
|---|---|
| Bit 5 | This status bit indicates the present state of clear channel assessment (CCA) which is output pin 32. The CCA is being asserted as a result of a channel energy monitoring algorithm that is a function of RSSI, carrier sense, and time out counters that monitor the channel activity. |
| Bit 4 | This status bit, when active indicates Carrier Sense, or PN lock.<br>Logic 1: Carrier present.<br>Logic 0: No Carrier Sense. |
| Bit 3 | This status bit indicates whether the RSSI signal is above or below the programmed RSSI 6-bit threshold setting. This signal is referred as Energy Detect (ED).<br>Logic 1: RSSI is above the programmed threshold setting.<br>Logic 0: RSSI is below the programmed threshold setting. |
| Bit 2 | This bit indicates the status of the output control pin MD_RDY (pin 34). It signals that a valid Preamble/Header has been received and that the next available bit on the TXD bus will be the first data packet bit.<br>Logic 1: Envelopes the data packet as it becomes available on pin 3 (TXD).<br>Logic 0: No data packet on TXD serial bus. |
| Bit 1 | This status bit indicates whether the external device has acknowledged that the channel is clear for transmission. This is the same as the input signal TX_PE on pin 2.<br>Logic 1 = Acknowledgment that channel is clear to transmit.<br>Logic 0 = Channel is NOT clear to transmit. |
| Bit 0 | This status bit indicates that a valid CRC16 has been calculated. The CRC16 is calculated on the Header information. The CRC16 does not cover the preamble bits.<br>Logic 1 = Valid CRC16 check.<br>Logic 0 = Invalid CRC16 check. |

**CONFIGURATION REGISTER 8 ADDRESS (20h) MODEM STATUS REGISTER B**

| | |
|---|---|
| Bit 7 | This status bit is meaningful only when the device operates under the full protocol mode. Errors imply CRC errors of the header fields.<br>Logic 0 = Valid packet received.<br>Logic 1 = Errors in received packet. |
| Bit 6 | This bit is used to indicate the status of the SFD search timer. The device monitors the incoming Header for the SFD. If the timer, times out the HSP3824 returns to its signal acquisition mode looking to detect the next Preamble and Header.<br>Logic 1 = SFD not found, return to signal acquisition mode.<br>Logic 0 = No time out during SFD search. |
| Bit 5 | This status bit is used to indicate the modulation type for the data packet. This signal is generated by the header detection circuitry in the receive interface.<br>Logic 0 = DBPSK.<br>Logic 1 = DQPSK. |
| Bit 4 | Unused, don't care. |
| Bit 3 | Unused, don't care. |
| Bit 2 | Unused, don't care. |
| Bit 1 | Unused, don't care. |
| Bit 0 | Unused, don't care. |

**CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER**

| | |
|---|---|
| | This register is used to define the phase of clocks and other interface signals. |
| Bit 7 | This bit needs to always be set to logic 0. |
| Bit 6 | This control bit selects the active level of the MD_RDY output pin 34.<br>Logic 1 = MD_RDY is active 0.<br>Logic 0 = MD_RDY is active 1. |

**CONFIGURATION REGISTER 9 ADDRESS (24h) I/O DEFINITION REGISTER**

| | |
|---|---|
| Bit 5 | This control bit selects the active level of the Clear Channel Assessment (CCA) output pin 32.<br>Logic 1 = CCA active 1.<br>Logic 0 = CCA active 0. |
| Bit 4 | This control bit selects the active level of the Energy Detect (ED) output which is an output pin at the test port, pin 45.<br>Logic 1 = ED active 0.<br>Logic 0 = ED active 1. |
| Bit 3 | This control bit selects the active level of the Carrier Sense (CRS) output pin which is an output pin at the test port, pin 46.<br>Logic 1 = CRS active 0.<br>Logic 0 = CRS active 1. |
| Bit 2 | This control bit selects the active level of the transmit ready (TX_RDY) output pin 5.<br>Logic 1 = TX_RDY active 0.<br>Logic 0 = TX_RDY active 1. |
| Bit 1 | This control bit selects the active level of the transmit enable (TX_PE) input pin 2.<br>Logic 1 = TX_PE active 0.<br>Logic 0 = TX_PE active 1. |
| Bit 0 | This control bit selects the phase of the transmit output clock (TXCLK) pin 4.<br>Logic 1 = Inverted TXCLK.<br>Logic 0 = NON-Inverted TXCLK |

**CONFIGURATION REGISTER 10 ADDRESS (28h) RSSI VALUE REGISTER**

Bits 0 - 7

This is a read only register reporting the value of the RSSI analog input signal from the on chip 6-bit ADC. This register is updated at (chip rate/11). Bits 7 and 6 are not used and set to Logic 0.
Example:

| | BITS (0:7) | RANGE |
|---|---|---|
| RSSI_STAT | 7 6 5 4 3 2 1 0 | |
| | 0 0 0 0 0 0 0 0 | 00h (Min) |
| | 0 0 1 1 1 1 1 1 | 3Fh (Max) |

**CONFIGURATION REGISTER 11 ADDRESS (2ch) A/D CAL POS REGISTER**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit control register contains a binary value used for positive increment for the level adjusting circuit of the A/D reference. The larger the step the faster the level reaches saturation. |

**CONFIGURATION REGISTER 12 ADDRESS (30h) A/D CAL NEG REGISTER**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit control register contains a binary value used for the negative increment for the level adjusting reference of the A/D. The number is programmed as 256 - the value wanted since it is a negative number. |

**CONFIGURATION REGISTER 13 ADDRESS (34h) TX SPREAD SEQUENCE (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is programmed with the upper byte of the transmit spreading code. This code is used for both the I and Q signalling paths of the transmitter. This register combined with the lower byte TX_SPREAD(LOW) generates a transmit spreading code programmable up to 16-bits. Code lengths permitted are 11, 13, 15, and 16. Right justified MSB first. |

**CONFIGURATION REGISTER 14 ADDRESS (38h) TX SPREAD SEQUENCE (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is programmed with the lower byte of the transmit spreading code. This code is used for the I and Q signalling paths of the transmitter. This register combined with the higher byte TX_SPREAD(HIGH) generates the transmit spreading code programmable up to 16-bits.<br>The example below illustrates the bit positioning for one of the 11-bit Barker PN codes.<br>Example:<br>Transmit Spreading Code 11-Bit Barker Word Right Justified MSB First. |

| | MSB | LSB |
|---|---|---|
| TX_SPREAD(HIGH) | 15 14 13 12 11 10 9 8 | |
| TX_SPREAD(LOW) | | 7 6 5 4 3 2 1 0 |
| 11-bit Barker code | X X X X X 1 0 1 | 1 0 1 1 1 0 0 0 |

**CONFIGURATION REGISTER 15 ADDRESS (3Ch) SCRAMBLER SEED**

| | |
|---|---|
| Bits 0 - 7 | This register contains the 7-bit (seed) value for the transmit scrambler which is used to preset the transmit scrambler to a known starting state. The MSB bit position (7) is unused and must be programmed to a Logic 0. The example below illustrates the bit positioning of seed. |

**CONFIGURATION REGISTER 16 ADDRESS (40h) SCRAMBLER TAP**

| | |
|---|---|
| Bits 0 - 7 | This register is used to configure the transmit scrambler with a 7-bit polynomial tap configuration. The transmit scrambler is a 7-bit shift register, with 7 configurable taps. A logic 1 is the respective bit position enables that particular tap. The MSB bit 7 is not used and it is set to a Logic 0. The example below illustrates the register configuration for the polynomial $F(x) = 1 + X^{-4}+X^{-7}$. Each clock is a shift left |

| | | LSB |
|---|---|---|
| Bits (0:7) | | 7 6 5 4 3 2 1 0 |
| | | $XZ^{-7}Z^{-6}Z^{-5}Z^{-4}Z^{-3}Z^{-2}Z^{-1}$ |
| Scrambler Taps | $F(x) = 1 + X^{-4}+X^{-7}$ | 0 1 0 0 1 0 0 0 |

**CONFIGURATION REGISTER 17 ADDRESS (44h)CCA TIMER THRESHOLD**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is used to configure the period of the time-out threshold of the CCA watchdog timer. If the channel is busy the timer counts until it reaches the programmed value and at that point it declares that the channel is clear independent of the actual energy measured within the channel. This register is programmable up to 8-bits.<br><br>$\text{Time (ms)} = 1000 \bullet \frac{N \bullet 5632}{\text{Chip Rate}}$, where N is the programmable value of CR17.<br><br>For example, for a chip rate of 11 MCPS and a desired timeout of ~11ms, N = 2ch. |

| | LSB | |
|---|---|---|
| Bits (0:7) | 7 6 5 4 3 2 1 0 | |
| | 0 0 0 0 0 0 1 0 | 02h (Min) |
| CCA_TIMER_TH | 1 1 1 1 1 1 1 1 | FFh (Max) |

**CONFIGURATION REGISTER 18 ADDRESS (48h) CCA CYCLE THRESHOLD**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is used to configure how many times the CCA timer is allowed to reach its maximum count before the channel is declared clear for transmission independent of the actual energy in the channel. This is an outer counter loop of the CCA timer. Each increment represents a time out of the CCA timer. Use a value of 03h for a time out of 2 CCA timer counts. |

| | MSB LSB | |
|---|---|---|
| Bits (0:7) | 7 6 5 4 3 2 1 0 | |
| | 0 0 0 0 0 0 1 0 | 2h; 1 CCA timer (Min) |
| CCA_TIMER_TH | 1 1 1 1 1 1 1 1 | FFh; 256 CCA timer (Max) |

**CONFIGURATION REGISTER 19 ADDRESS (4Ch) RSSI THRESHOLD, ENERGY DETECT**

| | |
|---|---|
| Bits 0 - 7 | This register contains the value for the RSSI threshold for measuring and generating energy detect (ED). When the RSSI exceeds the threshold ED is declared. ED indicates the presence of energy in the channel. The threshold that activates ED is programmable. Bits 7 an 6 of this register are not used and set to Logic 0. |

| | MSB LSB | |
|---|---|---|
| Bits (0:7) | 7 6 5 4 3 2 1 0 | |
| | 0 0 0 0 0 0 0 0 | 00h (Min) |
| RSSI_STAT | 0 0 1 1 1 1 1 1 | 3Fh (Max) |

**CONFIGURATION REGISTER 20 ADDRESS (50h) RX SPREAD SEQUENCE (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is programmed with the upper byte of the receive despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the lower byte RX_SPRED(LOW) generates a receive despreading code programmable up to 16-bits. Right justified MSB first. See address 13 and 14 for example. |

**CONFIGURATION REGISTER 21 ADDRESS (54h) RX SPREAD SEQUENCE (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is programmed with the lower byte of the receiver despreading code. This code is used for both the I and Q signalling paths of the receiver. This register combined with the upper byte RX_SPRED(HIGH) generates a receive despreading code programmable up to 16-bits. |

**CONFIGURATION REGISTER 22 ADDRESS (58h) RX SIGNAL QUALITY 1 ACQ (HIGH) THRESHOLD**

| | |
|---|---|
| Bits 0 - 7 | This control register contains the upper byte bits (8 - 14) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements made during acquisition at each antenna dwell. This threshold comparison is added with the SQ2 threshold in registers 30 and 31 for acquisition. A lower value on this threshold will increase the probability of detection and the probability of false alarm. Set the threshold according to instructions in the text. |

**CONFIGURATION REGISTER 23 ADDRESS (5Ch) RX SIGNAL QUALITY 1 ACQ THRESHOLD (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for acquisition. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurement made during acquisition at each antenna dwell. |

**CONFIGURATION REGISTER 24 ADDRESS (60h) RX SIGNAL QUALITY 1 ACQ READ (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This status register contains the upper byte bits (8 - 14) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the lower byte represents a 15-bit value, representing the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna. |

**CONFIGURATION REGISTER 25 ADDRESS (64h) RX SIGNAL QUALITY 1 ACQ READ (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the lower byte bits (0 - 7) of the measured signal quality threshold for the bit sync amplitude used for acquisition. This register combined with the higher byte represents a 15-bit value, of the measured bit sync amplitude. This measurement is made at each antenna dwell and is the result of the best antenna. |

**CONFIGURATION REGISTER 26 ADDRESS (68h) RX SIGNAL QUALITY 1 DATA THRESHOLD (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This control register contains the upper byte bits (8-14) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the lower byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols. These thresholds set the drop lock probability. A higher value will increase the probability of dropping lock. |

**CONFIGURATION REGISTER ADDRESS 27 (6Ch) RX SIGNAL QUALITY 1 DATA THRESHOLD (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This control register contains the lower byte bits (0 - 7) of the bit sync amplitude signal quality threshold used for drop lock decisions. This register combined with the upper byte represents a 15-bit threshold value for the bit sync amplitude signal quality measurements, made every 128 symbols. |

**CONFIGURATION REGISTER 28 ADDRESS (70h) RX SIGNAL QUALITY 1 DATA (high) THRESHOLD READ (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This status register contains the upper byte bits (8-14) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 15-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols. |

**CONFIGURATION REGISTER 29 ADDRESS (74h) RX SIGNAL QUALITY 1 DATA THRESHOLD READ (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the lower byte bits (0-7) of the measured signal quality of bit sync amplitude used for drop lock decisions. This register combined with the lower byte represents a 16-bit value, representing the measured signal quality for the bit sync amplitude. This measurement is made every 128 symbols. |

**CONFIGURATION REGISTER 30 ADDRESS (78h) RX SIGNAL QUALITY 2 ACQ THRESHOLD (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This control register contains the upper byte bits (8-15) of the carrier phase variance threshold used for acquisition. This register combined with the lower byte represents a 16-bit threshold value for carrier phase variance measurement made during acquisition at each antenna dwell and is based on the choice of the best antenna. This threshold is used with the bit sync threshold in registers 22 and 23 to declare acquisition. A higher value in this threshold will increase the probability of acquisition and false alarm. |

**CONFIGURATION REGISTER 31 ADDRESS (7Ch) RX SIGNAL QUALITY 2 ACQ THRESHOLD (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This control register contains the lower byte bits (0-7) of the carrier phase variance threshold used for acquisition. |

**CONFIGURATION REGISTER 33 ADDRESS (84h) RX SIGNAL QUALITY 2 ACQ READ (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This status register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance used for acquisition. This register combined with the lower byte generates a 16-bit value, representing the measured signal quality of the carrier phase variance. This measurement is made during acquisition at each antenna dwell and is based on the selected best antenna |

**CONFIGURATION REGISTER 34 ADDRESS (88h) RX SIGNAL QUALITY 2 DATA THRESHOLD (HIGH)**

| | |
|---|---|
| Bits 0-7 | This control register contains the upper byte bits (8-15) of the carrier phase variance threshold. This register combined with the lower byte represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols. |

**CONFIGURATION REGISTER 35 ADDRESS (8Ch) RX SIGNAL QUALITY 2 DATA THRESHOLD (LOW)**

| | |
|---|---|
| Bits 0-7 | This control register contains the lower byte bits (0-7) of the carrier phase variance threshold. This register combined with the upper byte) represents a 16-bit threshold value for the carrier phase variance signal quality measurements made every 128 symbols. |

**CONFIGURATION REGISTER 36 ADDRESS (90h) RX SIGNAL QUALITY 2 DATA READ (HIGH)**

| | |
|---|---|
| Bits 0-7 | This status register contains the upper byte bits (8-15) of the measured signal quality of the carrier phase variance. This register combined with the lower byte represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols. |

**CONFIGURATION REGISTER 37 ADDRESS (94h) RX SIGNAL QUALITY 2 DATA READ (LOW)**

| | |
|---|---|
| Bits 0-7 | This register contains the lower byte bits (0-7) of the measured signal quality of the carrier phase variance. This register combined with the represents a 16-bit value, of the measured carrier phase variance. This measurement is made every 128 symbols. |

**CONFIGURATION REGISTER ADDRESS 38 (98h) RX SIGNAL QUALITY 8-BIT READ**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the bit sync amplitude signal quality measurement derived from the 16-bit Bit Sync signal quality value stored in the CR28-29 registers. This value is the result of the signal quality measurement for the best antenna dwell. The signal quality measurement provides 256 levels of signal to noise measurement. |

**CONFIGURATION REGISTER 39 ADDRESS RESERVED**

| | |
|---|---|
| | Reserved |

**CONFIGURATION REGISTER 40 ADDRESS RESERVED**

| | |
|---|---|
| | Reserved |

**CONFIGURATION REGISTER 41 ADDRESS (A4h) SFD SEARCH TIME**

| | |
|---|---|
| Bits 0 - 7 | This register is programmed with an 8-bit value which represents the length of time for the demodulator to search for a SFD in a receive Header. Each bit increment represents 1 symbol period. |

**CONFIGURATION REGISTER 42 ADDRESS (A8h) DSBPSK SIGNAL**

| | |
|---|---|
| Bits 0 - 7 | This register contains an 8-bit value indicating the data packet modulation is DBPSK. This value will be a OAH for full protocol operation at a data rate of 1 MBPS, and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received Header. |

**CONFIGURATION REGISTER 43 ADDRESS (ACh) DQPSK SIGNAL**

| | |
|---|---|
| Bits 0 - 7 | This register contains the 8-bit value indicating the data packet modulation is DQPSK. This value will be a 14h for full protocol operation at a data rate of 2 MBPS and is used in the transmitted Signalling Field of the header. This value will also be used for detecting the modulation type on the received header. |

**CONFIGURATION REGISTER 44 ADDRESS (B0h) RX SERVICE FIELD (RESERVED)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the detected received 8-bit value of the Service Field for the Header. This field is reserved for the full protocol mode for future use and should be always a 00h. |

**CONFIGURATION REGISTER 45 ADDRESS (B4h) RX DATA LENGTH (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the detected higher byte (bits 8-15) of the received Length Field contained in the Header. This byte combined with the lower byte indicates the number of transmitted bits in the data packet. |

**CONFIGURATION REGISTER 46 ADDRESS (B8h) RX DATA LENGTH (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the detected lower byte of the received Length Field contained in the Header. This byte combined with the upper byte indicates the number of transmitted bits in the data packet. |

**CONFIGURATION REGISTER 47 ADDRESS (BCh) RX CRC16 (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the upper byte bits (8 -15) of the received CRC16 field Header. This register combined with the lower byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2. |

**CONFIGURATION REGISTER 48 ADDRESS (C0h) RX CRC16 (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This register contains the lower byte bits (0-7) of the received CRC16 field Header. This register combined with the upper byte represents a 16-bit CRC16 value protecting transmitted header. The fields protected are selected by configuring the header control bits at configuration register 2. |

| | **MSB** **LSB** |
|---|---|
| RX_CRC16 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| RX_CRC16(HIGH) | 7 6 5 4 3 2 1 0 |
| RX_CRC16(LOW) | 7 6 5 4 3 2 1 0 |

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection, as defined in configuration register 2.

Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

**CONFIGURATION REGISTER 49 ADDRESS (C4h) SFD (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the upper byte bits (8-15) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field. |

**CONFIGURATION REGISTER 50 ADDRESS (C8h) SFD (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the upper byte bits (0-7) of the SFD used for both the Transmit and Receive header. This register combined with the lower byte represents the 16-bit value for the SFD field. |

**CONFIGURATION REGISTER 51 ADDRESS (CCh) TX SERVICE FIELD**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register is programmed with the 8-bit value of the Service Field to be transmitted in a Header. This field is reserved for future use and should be always a 00h. |

**CONFIGURATION REGISTER 52 ADDRESS (D0h) TX DATA LENGTH FIELD (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the higher byte (bits 8-15) of the transmit Length Field described in the Header. This byte combined with the lower byte indicates the number of bits to be transmitted in the data packet. CR 52/53 should not be set to 0000h. This value would cause the modem to reset after SFD. |

**CONFIGURATION REGISTER 53 ADDRESS (D4h) TX DATA LENGTH FIELD (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the lower byte bits (0-7) of the transmit Length Field described in the Header. This byte combined with the higher byte indicates the number of bits to be transmitted in the data packet, including the MAC payload header. CR 52/53 should not be set to 0000h. This value would cause the modem to reset after SFD. |

**CONFIGURATION REGISTER 54 ADDRESS (D8h) TX CRC16 (HIGH)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the upper byte (bits 8-15) of the transmitted CRC16 Field for the Header. This register combined with the lower byte represents a 16-bit CRC16 value calculated by the HSP3824 to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02. |

**CONFIGURATION REGISTER 55 ADDRESS (DCh) TX CRC16 (LOW)**

| | |
|---|---|
| Bits 0 - 7 | This 8-bit register contains the lower byte (bits 0-7) of the transmitted CRC16 Field for the Header. This register combined with the higher byte represents a 16-bit CRC16 value calculated by the HSP3824 to protect the transmitted header. The fields protected are selected by configuring the header mode control bits at register address 02. |

configuration register 2

| | MSB LSB |
|---|---|
| RX_CRC16 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| RX_CRC16(HIGH) | 7 6 5 4 3 2 1 0 |
| RX_CRC16(LOW) | 7 6 5 4 3 2 1 0 |

NOTE: The receive CRC16 Field protects the following fields depending upon the mode selection. as defined in register address 02.

Mode 0 CRC16 not used
Mode 1 CRC16 protects SFD
Mode 2 CRC16 protects SFD, and Length Field
Mode 3 CRC16 protects Signalling Field, Service Field, and Length Field

**CONFIGURATION REGISTER 56 ADDRESS (E0h) TX PREAMBLE LENGTH**

| | |
|---|---|
| Bits 0 - 7 | This register contains the count for the Preamble length counter. This counter is programmable up to 8-bits and represents the number of preamble bits. This should be set at 50h for 1 antenna and 80h for dual antennas. |

## *Sales Office Headquarters*

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

**NORTH AMERICA**
Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

**EUROPE**
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

HARRIS SEMICONDUCTOR