

PLL Hardware Design and Software Simulation using the 16-bit version of SystemView by ELANIX

Stephen Kratzet, Elanix, Inc.

Introduction

This application note describes the design of a phased locked loop (PLL). The design begins with a small breadboard to document the voltage controlled oscillator's (VCO) transfer function, then the component values for the loop filter are calculated. The design is then verified by completing the breadboard. Software simulation of the breadboard is described using SystemView by ELANIX, and the results of the simulation are compared with the operation of the breadboard.

A brief description of this particular phase locked loop (**Figure 1**) follows. The frequency output from the VCO is divided-by-4 and compared to an accurate and stable reference frequency. The output of the Phase/Frequency Detector and Filter/Integrator combination adjusts the VCO as necessary (up or down in frequency) to cause the R and V inputs to be at the same frequency and in phase with each other. Variations of this loop include, a division factor other than 4, an additional divider at the output of the VCO, and/or a divider between the Ref. Freq. and the R input. The digital phase/freq. detector is by its nature a sampled function. Its output is not an analog continuous signal. It can make a correction only once each cycle of the reference input. One of the jobs of the filter is to reduce this sample frequency to an amplitude low enough to provide an acceptable low jitter VCO output, while at the same time provide a loop response time quick enough for the intended application. (Not shown in the block diagram, is the requirement to shift the voltage level of the VCO output to one acceptable to the input of the counter.)

Breadboarding the VCO

Start the design with the most constrained part, the VCO. Analog VCO's generally have a non-linear transfer function, over a narrow output frequency span. The highest output frequency is about 2 1/2 times the lowest output frequency. The VCO used in this example is the Motorola MC1648P. Motorola's data book has some useful example circuits along with graphs of their transfer functions (**Ref. 1**). The schematic in **Figure 2** shows the oscillator tank circuit is comprised of a pair of MV1404 varactor diodes and a 2.4 uH inductor. The value of the inductor was selected with the help of a MICROMETALS catalog "Q CURVES for iron cores". The Q curves on page 21 indicate that a MICROMETALS T 27-6 toroid has the following characteristics:

Number of turns	AWG	Inductance	Peak Q	Freq. at peak Q
32	30	2.70 uH	156	9.0 MHz
25	28	1.65 uH	190	14.0 MHz

Table 1. Parameters for a T27-6 Toroid.

Because the desired center frequency of the VCO was close to 12 MHz, the toroid was wound with 30 turns of AWG 30 wire. (Fewer turns could have been used, also.)

The inductance of a toroid is proportional to the number-of-turns squared. Therefore, (with the toroid inductance tolerances being +/- 5%):

$$\frac{32^2 \text{ turns}}{2.7 \mu\text{H}} = \frac{30^2 \text{ turns}}{L}$$

therefore $L = 2.4 \mu\text{H}$

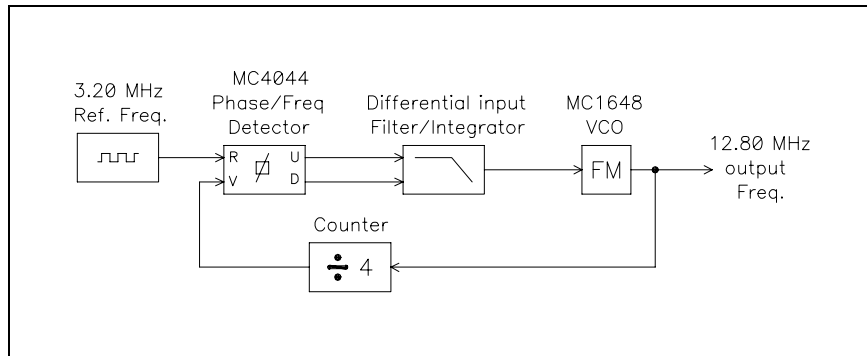


Figure 1. Phase Locked Loop block diagram

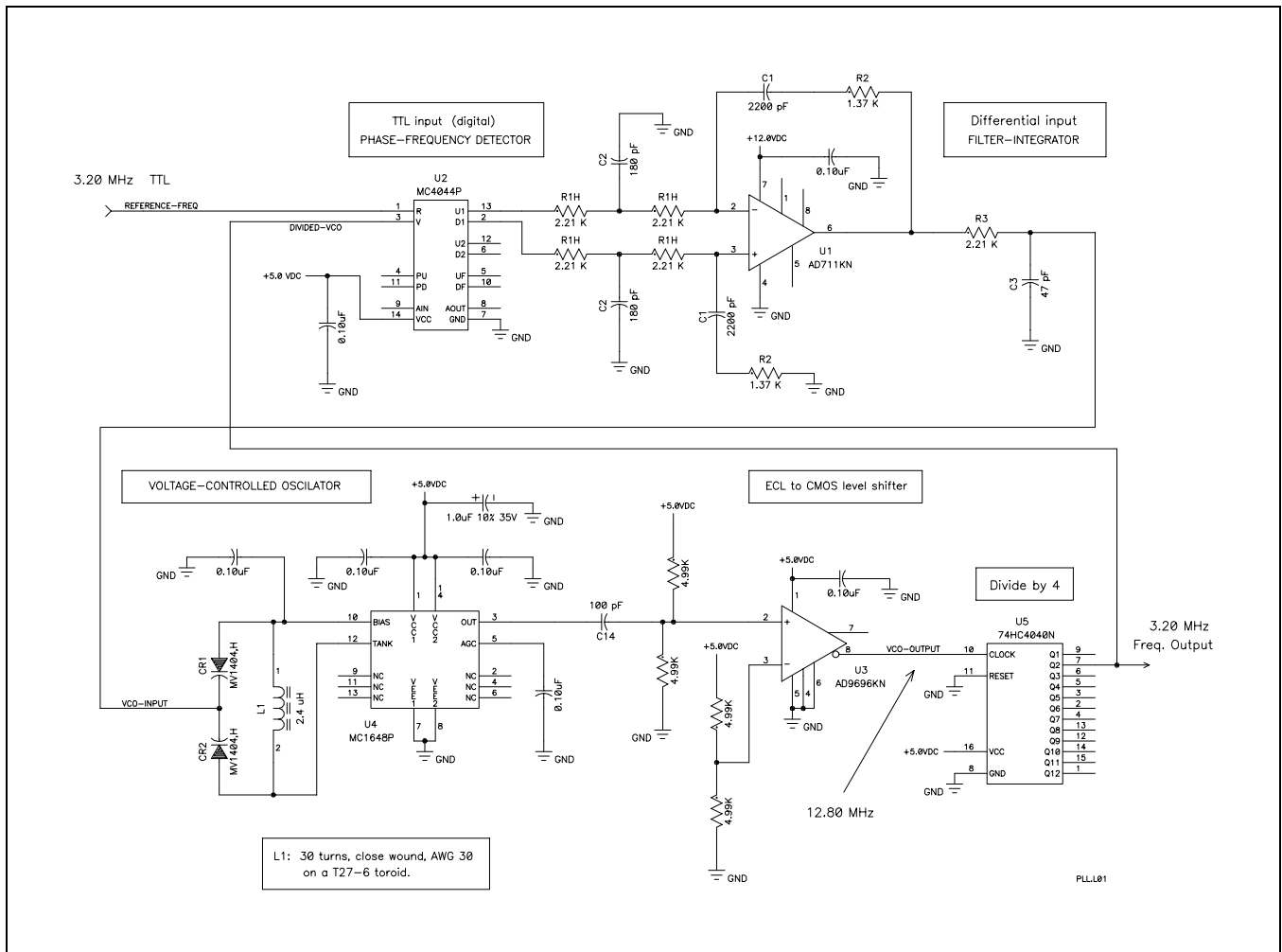


Figure 2. Schematic of the Phase Locked Loop circuit breadboard.

Just the MC1648P portion of the circuit was measured on the breadboard. The VCO transfer function is shown in **Table 2** and **Figure 3**.

Input voltage (volts)	Output freq. (MHz)
0.5	5.87
1.0	6.40
1.5	7.45
2.0	8.37
2.5	9.17
3.0	9.89
3.5	10.60
4.0	11.40
4.5	12.30
5.0	13.30
5.5	14.50
6.0	15.80
6.5	17.30
7.0	18.90
7.5	20.70
8.0	22.60
8.5	24.90
9.0	26.80
9.5	27.70
10.0	28.00

Table 2. Measured transfer function of the VCO (MC1648P) breadboard.

values=20
min=0.5
max=10
-3.48
-3.24
-2.78
-2.37
-2.01
-1.69
-1.38
-1.02
-0.62
-0.18
0.36
0.93
1.60
2.31
3.11
3.96
4.98
5.82
6.22
6.36

Table 3. Format of the file "TF-FM.TXT" for the Xfer Fct token.

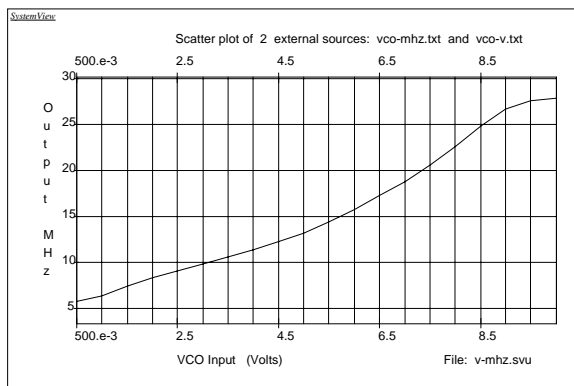


Figure 3. Graph of the VCO transfer function in Table 2.

Types of Phase Detectors

There are three types of phase detectors (**Ref. 2**).

1. Analog or multiplier (mixer).
2. Exclusive-OR.
(The digital equivalent of the analog multiplier).
3. Digital phase-frequency detector (CD4046 or MC4044 type).

The main advantage of the analog phase detector is its ability to recover a signal from a low signal-to-noise input. Unfortunately, it will also lock in on harmonics of the desired input. For the noise free TTL signals found in a frequency synthesizer, the third type of phase detector is a better choice. The MC4044 responds only to the falling edges of the inputs, eliminating the harmonics lock-in problem. The CD4046 responds to the rising edges only. The digital phase detector is not perfect, an extra or missing pulse generates a large error for a short time. Also, it is important, with the MC4044, to maintain the correct polarity when connecting the U1 and D1 outputs of the digital Phase/Freq. detector to the differential inputs of the integrator. (It does not matter which output of the analog comparator, inverted or non-inverted, is connected to the counter's clock input.)

The Differential Input Filter / Integrator

There are many types of filters that can be used in a PLL. For the MC4044 (**Ref. 3**), the differential input op-amp integrator can provide superior performance. One advantage is that the differential input allows the integrator to have a separate ground from the digital Phase/Freq. detector ground. The filter is comprised of 5 parts: (See **Figure 2**.)

- A. The main integrator R1 and C1.
(Where $R1 = 2 \times R1h$)
- B. The corner frequency at which the integrator reverts to a constant loss R2, C1.
- C. The maximum loss after the corner frequency: $R2 / R1$.
- D. A "tee" pre-filter R1h, C2, R1h.
- E. A varactor filter R3, C3.

The "tee" filter integrates the U1 and D1 signals to allow the op-amp to operate more accurately on the error information in the very narrow U1 and D1 pulse widths. This results in better sideband filtering. The cutoff frequency of the varactor filter is made high enough so it has almost no effect on the loop bandwidth. It also provides a convenient place to break the loop for open loop testing.

Differential Input Filter / Integrator -- Selected Operating Conditions

Capacitor C1 is selected to obtain reasonable resistor values for the op-amp circuit. BWp determines the loop lock-up time, and it can be fine tuned to adjust at least some of the resistors to be close to standard values. The damping factor (df) determines the amplitude of overshoot in response to a step input. The value of this factor is usually set between 1.0 (13% overshoot) and 0.5 (30% overshoot) for a Type 2, 2nd Order filter.

From the measurements in **Table 1**:

$$\begin{aligned} S_{vco} &= \Delta \text{MHz} / \Delta \text{volts} \\ &= (18.9\text{MHz} - 9.89\text{mhz}) / (7.0\text{v} - 3.0\text{v}) \\ &= 2.25 \text{ MHz/volt} \end{aligned}$$

$$\begin{aligned} f_o &= \sqrt{F_{\text{high}} \times F_{\text{low}}} \\ &= \sqrt{18.9\text{MHz} \times 9.89\text{MHz}} \\ &= 13.7 \text{ MHz} \end{aligned}$$

The two items above and the system constraints' results in the following 7 parameters that are used to calculate the component values of the loop filter (**Table 4**):

VDD	4.00	volts	Measured phase detector output voltage swing.
Svco	2.3E+6	Hz/volt	Measured VCO sensitivity.
C1	2.2E-9	farads	Selected value for the main integrator capacitor.
df	0.707		Selected damping factor (21 % overshoot).
fr	3.2E+6	Hz	Reference frequency input to the phase detector. (Channel spacing)
BWp	4.900	%	Selected loop bandwidth as a percentage of the ref. freq.
fo	13.7E+6	Hz	Approximate center frequency of the VCO.

Table 4. Seven parameters for the PLL calculations.

Filter Calculations based on the selected operating conditions

VCO gain constant:

$$\begin{aligned} K_{vco} &= 2 \times \text{Pi} \times S_{vco} \\ &= 14.14\text{e}+6 \text{ rad/sec/volt} \end{aligned}$$

Loop bandwidth in Hz:

$$B_{WHz} = B_{Wp} \times 0.01 \times f_r = 156,800 \text{ Hz}$$

Loop bandwidth in rad/sec:

$$B_{Ww} = 2 \times \text{PI} \times B_{WHz} = 985.20\text{e}+3 \text{ rad/sec}$$

Radical used to determine the filter's natural frequency:

$$\begin{aligned} \text{radical} &= \sqrt{d + \sqrt{d + 1}} = 2.1009 \\ (\text{where: } d &= (2 \times df^2) + 1 = 1.9997) \end{aligned}$$

Total reference frequency count:

$$\begin{aligned} N_t &= f_o / f_r \\ &= 4.28 \end{aligned}$$

The filter's natural frequency in Hz:

$$\begin{aligned} F_{NHz} &= B_{WHz} / \text{radical} \\ &= 74,634 \text{ Hz} \end{aligned}$$

The filter's natural freq. in radians/sec:

$$\begin{aligned} f_{Nw} &= 2 \times \text{Pi} \times f_{NHz} \\ &= 468,942 \text{ rad/sec} \end{aligned}$$

Phase detector gain constant:

$$\begin{aligned} K_{ph_det} &= V_{DD} / (2 \times \text{Pi}) \\ &= 0.637 \text{ volts/rad} \end{aligned}$$

Main integrator resistor (before being split):

$$\begin{aligned} R_1 &= (K_{ph_det} \times K_{vco}) / (C_1 \times f_{Nw}^2 \times N_t) \\ &= 4,345 \text{ ohms} \end{aligned}$$

Main integrator resistor (after being split):

$$\begin{aligned} R_{1h} &= R_1 / 2 \\ &= 2,173 \text{ ohms} \end{aligned}$$

The resistor in series with C1:

$$\begin{aligned} R_2 &= (2 \times df) / (f_{Nw} \times C_1) \\ &= 1,317 \text{ ohms} \end{aligned}$$

The input "tee" capacitor:

(Used 0.4 instead of Motorola's 0.8. If C2 gets too large, the loop tends to oscillate.)

$$\begin{aligned} C_2 &= 0.4 / (f_{Nw} \times R_1) \\ &= 196\text{e}-12 \text{ farads} \end{aligned}$$

The varactor filter resistor:

$$\begin{aligned} R_3 &= R_1 \\ &= 2,173 \text{ ohms} \end{aligned}$$

The varactor filter capacitor:

$$\begin{aligned} C_3 &= C_2 / 4 \\ &= 49.1\text{e}-12 \text{ farads} \end{aligned}$$

Figure 4 shows the bode plot of the integrator with just R1, R2, and C1 installed. It has a breakpoint at 60.5 kHz at which it reverts to a constant loss. The resulting loss after the breakpoint is:

$$R2 / (R1h \times 2) = 294 / (590 \times 2) = 0.249$$

$$\text{Expressed in dB: } 20 \log(0.249) = -12.07 \text{ dB}$$

Adding C2 (the "tee cap") to the circuit gives the integrator a 2nd breakpoint at 500 kHz (**Figure 5**). In both **Figures 4** and **5** the phase margin is displayed -- the frequency and phase at which the gain passes through 0 dB.

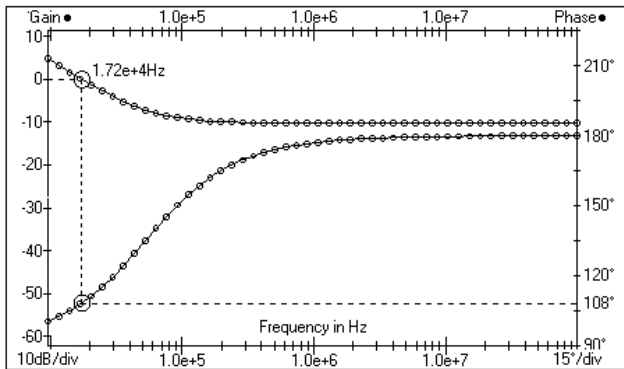


Figure 4. Bode plot of the integrator with 1 breakpoint, (without the "tee cap").

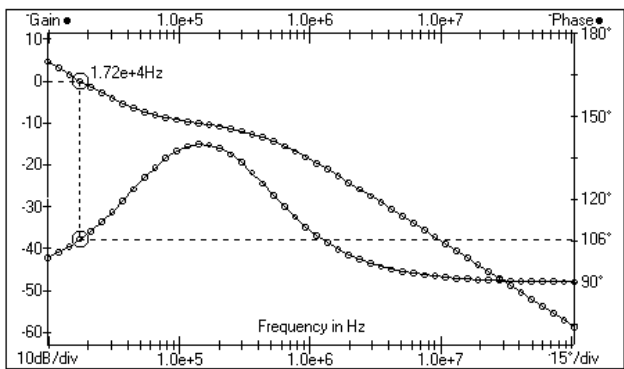


Figure 5. Bode plot of the integrator with 2 breakpoints, (with the "tee cap").

Simulating the VCO

SystemView by ELANIX was used to simulate the VCO transfer function in **Table 2**.

First, a linear VCO is defined by setting the parameters of an FM token (from the red Function Library) as follows:

- Amplitude (v) = 1 (default, zero-to-peak)
- Mod Gain (Hz/v) = 2.25e+6
- Frequency (Hz) = 13.7e+6
- Phase (deg) = 0 (default)

The Frequency, 13.7e+6, is fo, the center of the operating range of the VCO. The Mod Gain of 2.25e+6 is Svco, the measured VCO sensitivity. This FM token will now have the transfer function shown in **Table 5**.

Volts	MHz
etc.	etc.
-1.5	10.325
-1.0	11.450
-0.5	12.575
0.0	13.700
0.5	14.825
1.0	15.950
1.5	17.075
etc.	etc.

Table 5. The linear transfer function of the FM token.

The FM token's transfer function is made non-linear by preceding it with an External Transfer Function (Xtrnl Fct) token. This token performs a linear interpolation based on the input signal and the data in the external text file, shown in **Table 3**. The data in **Table 3** was calculated as follows:

$$(F_{out} - F_{center}) / 2.25 = (5.87 - 13.7) / 2.25 = -3.48$$

Referring to **Tables 2, 3, and 5**, the signal flow is as follows. A 0.5 volt input to the Xfer Fct token results in a -3.48 volt output. This is applied to the FM token that has a gain of 2.25 MHz/Volt and a center frequency of 13.7 MHz (zero volts input). The FM token will have an output of $(3.48 * 2.25)$ MHz less than the 13.7 MHz center frequency. $(13.7 - 7.83) = 5.87$ MHz)

To simulate ECL (emitter coupled logic) levels, the FM token's sinewave output is followed by a Limiter token and then a polynomial (Poly) token. The VCO simulation and results are shown in **Figures 6** and **7**. These four Function tokens will be contained in one Metasystem token and used as the VCO in a PLL simulation.

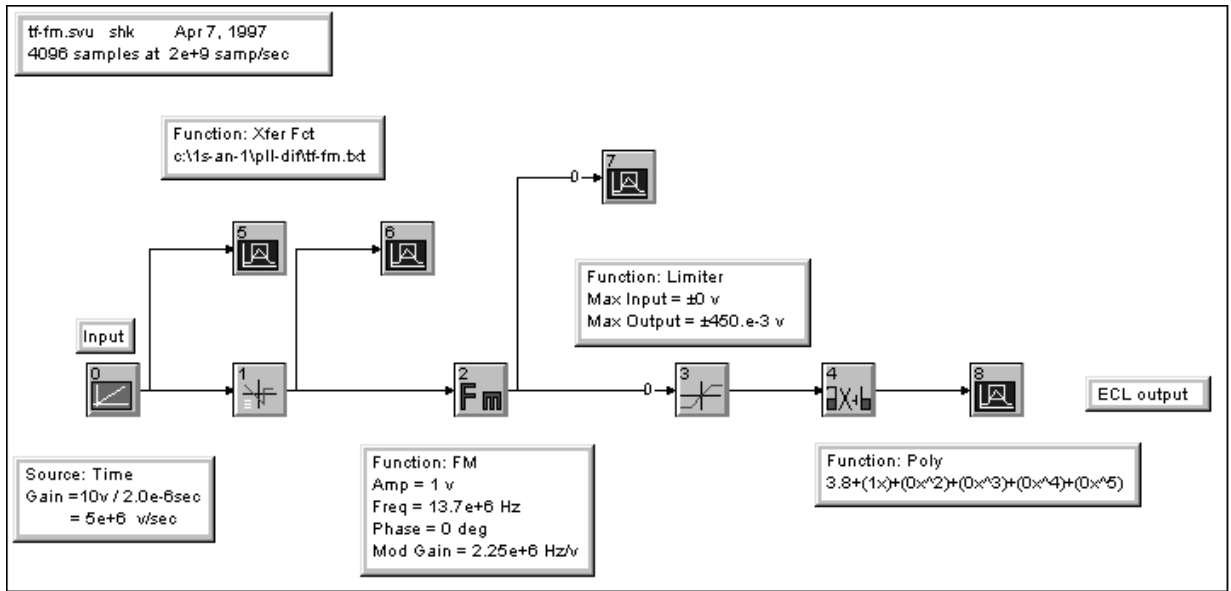


Figure 6. Test system for the VCO simulation.

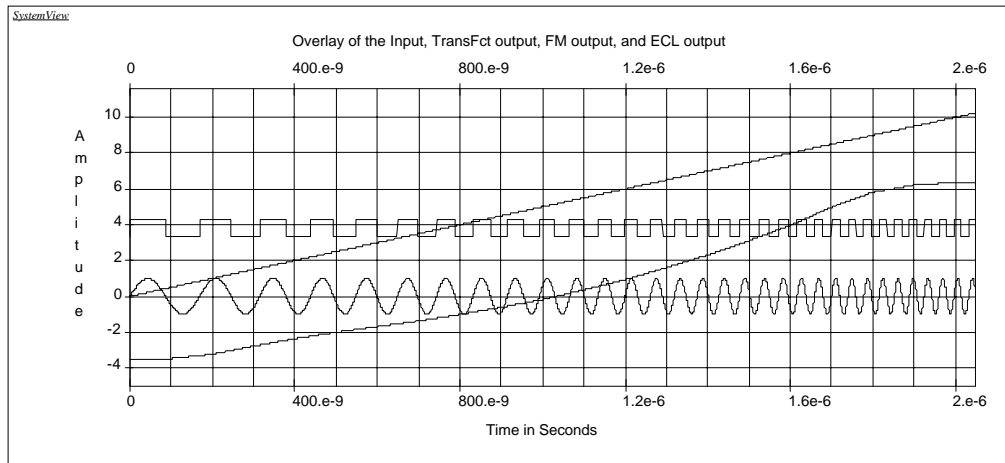


Figure 7. Input, transfer function, and output plots of the VCO simulation.
(4096 samples at 512e6 samples/sec)

Simulating the PLL breadboard

Figure 8 shows the PLL as it appears in the SystemView System window. The Op-Amp Integrator, and RC filters, are tokens from the RF Library. The Analog Comparator, Counter/Divider (744040), and the Phase Detector (MC4044), are from the Logic Library. All of the other tokens are from the standard library. **Figure 9** is a RC lowpass filter (PLL RC1) for the "tee filter". Notice that the PLL RC1 token is made into a 1-pole filter by assigning zero or very large parts values to the unused components. (This is not a true "tee filter", but the loop lockup time is practically unaffected.) **Figure 10** is the parameter entry window for the loop filter. A ground signal is connected to the Op Amps positive input using a Step source set to zero

volts. A 2nd RC lowpass filter (PLL RC1) is used for the varactor circuit, with $R = 2.21K$ and $C = 47pF$. **Figure 11** shows the parameter entry window for the RC highpass filter (RC Deriv) used in the ECL-to-TTL level shifter. **Figures 12** and **13** show a lock-in time of about 10 uSec with about 20% overshoot. During this time the VCO goes from its low frequency limit of 5.87 MHz to the locked-in frequency of 12.8 MHz. Oscilloscope measurements of the breadboard exhibited almost exactly the same sawtooth step response time and overshoot value. **Figure 14** shows the VCO output sweeping in frequency and locked-in with the 12.8 MHz spectral line a little above 0 dBm.

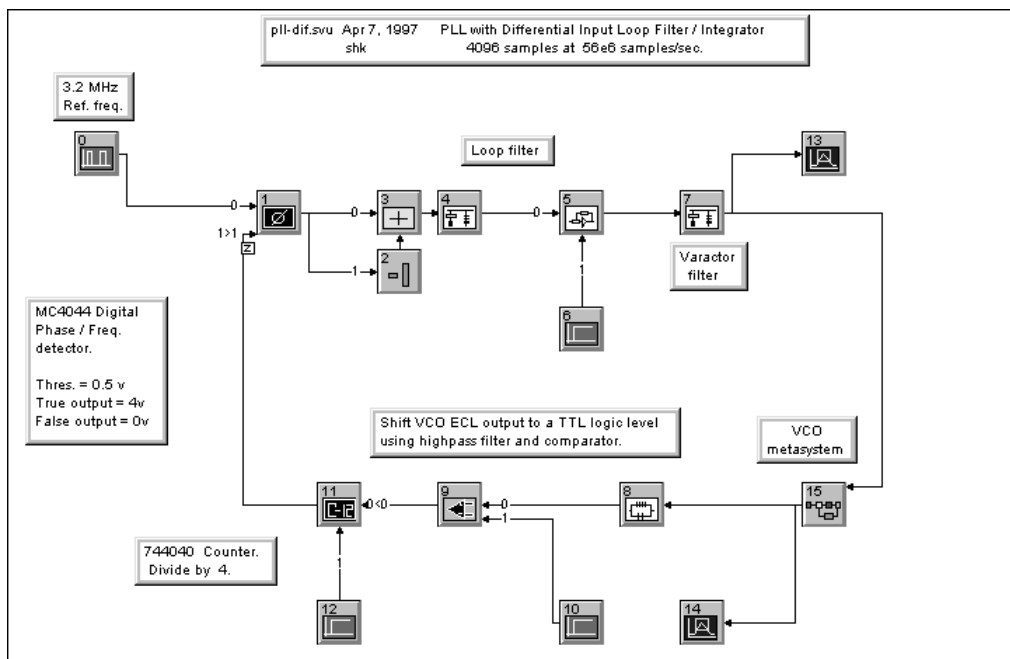


Figure 8. The PLL as it appears in SystemView's System window.

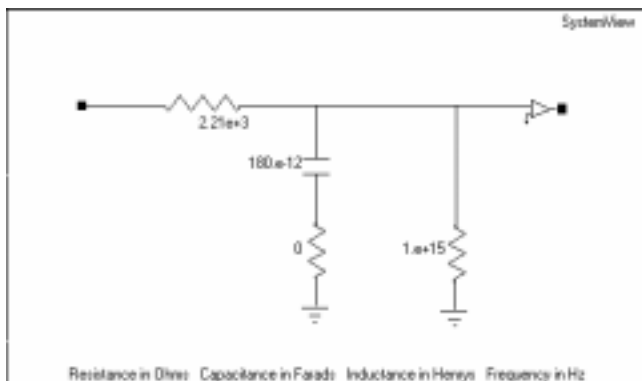


Figure 9. The PLL-RC1 parameter entry window, used for the "tee filter".

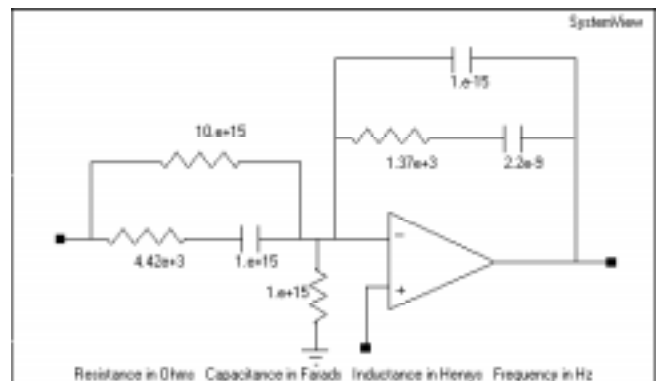


Figure 10. The Filter/Integrator (Op Amp) parameter entry window.

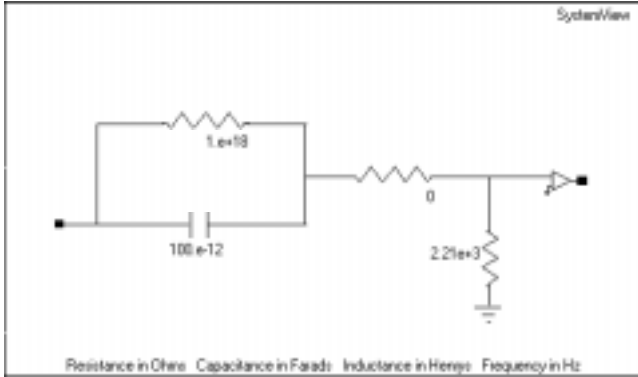


Figure 11. The RC Deriv parameter entry window, used as a 1-pole highpass filter, preceding the comparator.

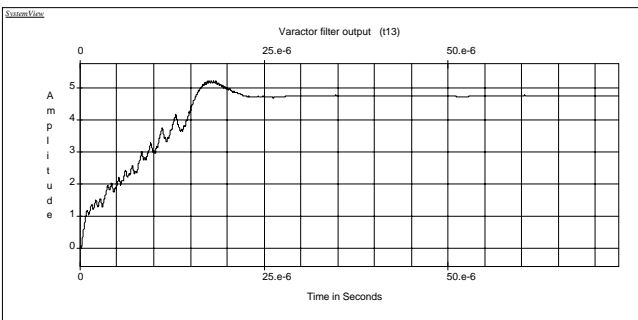


Figure 12. VCO increasing in frequency as the loop locks onto the Ref. frequency. (4096 samples at 56e6 samples/sec)

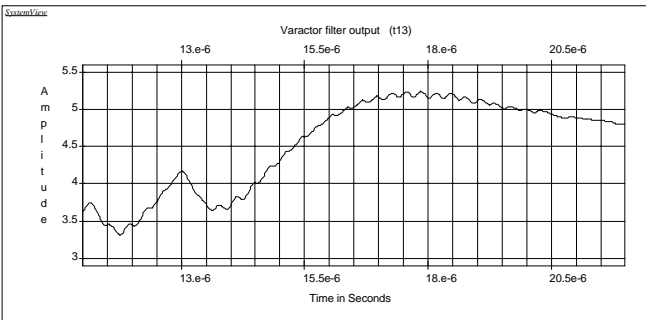


Figure 13. A "zoomed in" area of Figure 11, showing the overshoot.

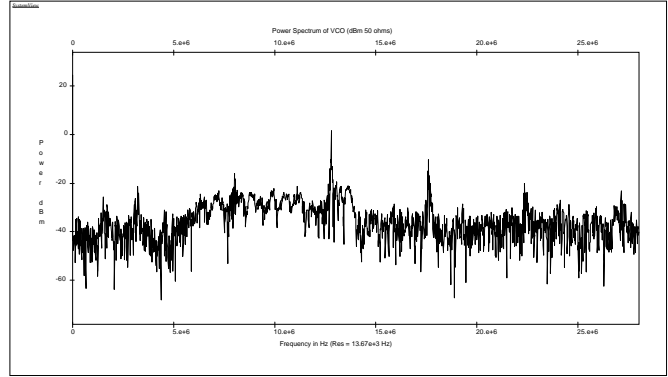


Figure 14. VCO increasing in frequency and locked in at 12.8 Mhz. (4096 samples at 56e6 samples/sec)

SystemView runs as a time sampled system. Nyquist's sampling theorem (**Ref. 4** and **Ref. 5**) would have us set the sample rate at a minimum of 2 x the maximum frequency. Since the highest frequency output of the VCO is about 14 MHz, including the overshoot, the minimum sample rate is 2 x 14 MHz yielding 28e6 samples/sec. The system sample rate used in this simulation is 56e6 samples/sec. This is 4 times the highest frequency in the system (14 MHz). A lower frequency sample rate will work (28e6 samples/sec), yielding a faster simulation, but the waveform plots are not as accurate. In this example, increasing the sample rate above 4 or 5 times the 14 MHz frequency does not seem to have any benefit.

In a future update of the RF Library the 5 tokens that comprise the loop filter (**Figure 8**) will be consolidated into one token.

Additional information on PLL's can be found in Alan Tam's article (**Ref. 6**), and Motorola's publications (**Ref. 7**, and **Ref. 8**).

An evaluation version of the software, SystemView by ELANIX, Inc., that will run the examples in this article is available on the Internet. Also, available is the spreadsheet PLL-DIF.XLS that calculates the PLL filter's parts values based on 7 entered parameters. The spreadsheet runs under Microsoft's EXCEL.

Summary

The software simulation of a PLL has been shown to closely match the measured response of a breadboard version of the PLL. This simulation enables the electronic system designer to try "what ifs" to gain further insights into the operation of a PLL. Also, a spreadsheet format for calculating the loop filter component values has been presented. Additional PLL simulation information is contained in application note --

AN103 Alias (Spur) Reduction in Sampled Systems using the 16-bit version of SystemView by ELANIX

References

1. MECL Data, DL122/D Rev 5, Motorola, pages 4-3 through 4-10, (MC1648).
2. Fred Salvatti, "Technique eases design of phase-locked loops" -- "A PLL primer", EDN, August 20, 1990
3. MECL Data, DL122/D Rev 5, Motorola, page 6-30, (MC4044).
4. Analog Devices, "MIXED-SIGNAL DESIGN SEMINAR, pages III-2 to III-4
5. Harris Semiconductor, "1994 HIGH SPEED SIGNAL PROCESSING SEMINAR", Glossary page 19, 24
6. Alan Tam, "A 180-MHz synthesizer from a \$10 CMOS chip", MICROWAVES & RF, Apr 1986
7. Radio, RF and Video Applications, DL413/D, Motorola, pages 56-66.
8. Application Note, AN532A, Motorola.

More Information

For more information on SystemView simulation software please contact:

ELANIX, Inc.
5655 Lindero Canyon Road, Suite 721
Westlake Village CA 91362.
Tel: (818) 597-1414
Fax: (818) 597-1427

Or visit our web home page (<http://www.elanix.com>) to download an evaluation version of the software that can these simulations as well as other user entered designs.